



- 2017 -

CALL FOR ABSTRACTS

September 14 - 15
Bangalore, India



DVCon India 2017

September 14-15, 2017 | The Leela Palace, Bangalore, India

Submission Deadline: April 25, 2017

The Design and Verification Conference & Exhibition India (DVCon India) is a highly technical conference in India targeting the application of standardized languages, tools and methodologies for the design and verification of electronic systems, embedded systems and integrated circuits. Hosted by Accellera Systems Initiative, the format of DVCon India is patterned on the successful DVCon United States conference held for over 10 years in the Silicon Valley.

The ultimate goal of DVCon India is to boost the interest, usage and development of electronic system designs. We look forward to users sharing the various challenges and solutions adopted by various teams across the industry. DVCon India also provides a much-needed platform to promote upcoming Electronic Design Automation (EDA) and Intellectual Property (IP) standards in India.

This 2-day conference is organized to invite industry practitioners to learn and share best practices on:

- Modeling, Design and Verification of complex electronic systems at different levels of abstraction such as Virtual prototyping, Architectural Modeling, RTL, Emulation, HW acceleration, etc.
- The application of system-level design and verification languages such as SystemC, SystemVerilog, PSL, e, VHDL etc for digital designs and Verilog-AMS for Analog Mixed Signal designs
- Virtual Platform for Embedded Software Development
- SoC Design Verification using the latest trends and methodologies such as UVM-SystemC, graph-based techniques, portable stimulus across block-subsystem-system all the way up to Post-Silicon
- Architectural Exploration at the early stage and High-level Synthesis
- The use of SystemVerilog Assertions (SVA), Property Specification Language Assertions (PSL) and Formal Verification Techniques (Model Checking)
- Adoption of Universal Verification Methodology (UVM)
- Leveraging on legacy methodologies based on OVM, VMM and migration to UVM
- IP reuse, design automation and integration standards based on IP-XACT and SystemRDL
- Low-power design and verification using the Unified Power Format (UPF)

General topic areas on Electronic System Level (ESL), Virtual Platform, Verification & Validation, Analog/Mixed-Signal, IP reuse, Design Automation, and Low-power design and verification will be highlighted in tutorials, papers, and poster sessions.

Conference attendees are primarily designers of embedded systems, electronic systems, ASICs and FPGAs, as well as those involved in the research, development and application of EDA tools and IP integration solutions. The DVCon India conference attracts a highly skilled user base active in various industries focusing on research and development of automotive, aerospace, consumer, medical, and wired and wireless communication products.

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Sponsor: Accellera Systems Initiative is an industry consortium with a mission to provide design and verification standards required by systems, semiconductor, IP, and design tool companies to enhance a front-end design automation process. Visit Accellera.org.

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Call for Abstracts — ESL Track

DVCon India solicits technically rich presentations that reflect real life experiences in using languages, standards, methods and Electronic Design Automation (EDA) tools.

The ESL track aims to accelerate the adoption of SystemC in the Semiconductor Industry. It provides a platform for the SystemC/TLM beginners and experts, ESL managers, and ESL vendors to share their knowledge, experiences and best practices about SystemC usage. Submissions are encouraged in (but not restricted to) the following topics:

- Transaction-level modeling for system-level design (VP, Multi-core, Performance, etc.)
- SystemC Language Development
- Verification Techniques using SystemC-UVM and VPI/PLI, DPI Interface
- Mixed-language environments involving SystemC and SystemVerilog/UVM
- SystemC Analog/Mixed-Signal Extensions & Power Modeling
- High-level synthesis using ESL languages SystemC/C++
- System-level design techniques, flows and methodologies
- Hardware/software/embedded co-design for early development
- HW/SW Co-Simulation and SoC Architecture Exploration
- Debugging Techniques and Configuration and Control in Platform Design

Important Deadlines

April 25, 2017	Abstract submission deadline
June 14, 2017	Accept/Reject Notification
July 14, 2017	Final paper due
August 7, 2017	Deadline to submit copyright form, and draft presentation slides due for review
September 1, 2017	Final presentation slides due for online proceedings

Call for Abstracts — DV Track

DVCon India solicits presentations that are highly technical and reflect real life experiences in using languages, standards, methods and Electronic Design Automation (EDA) tools for Design/Verification/Debug domains.

In the DV Track we are soliciting detailed abstracts from industry leaders to share their ideas, thoughts and experiences in solving some of the most complex challenges in their respective fields of work/research. This track provides a platform for the wide Design-Verification community including beginners, architects/experts, managers and EDA vendors to share their knowledge, experiences and best practices about Design-Verification. Submissions are encouraged in (but not restricted to) the following topics:

- Using multiple HDLs and/or HVLs in a design cycle
- Novel application of existing standard DV (Design-Verification) languages such as SystemVerilog, PSL, e, VHDL, etc.
- Latest language developments in SystemVerilog
- Advanced stimulus generation methods, reuse of stimulus across levels of pre/post silicon testing (portable stimulus)
- System-on-Chip (SoC) Verification approaches to handle complexity, performance and reusability requirements including HW/SW cosim environments
- UVM adoption, advanced techniques/features and extensions
- Real life applications of assertions using SVA and/or PSL
- Formal and semi-formal techniques, Assertion automation/synthesis
- Verification process and resource management
- Compliance and requirements-driven verification such as DO-254 standards
- Debug automation through transaction-level debug, smart tricks to handle simulation performance issues, faster time to debug techniques
- Low Power intent verification through standards such as UPF and related technologies
- Usage of IPXACT and SystemRDL in design flow
- AMS challenges in Verification, usage of custom extensions to UVM/SystemVerilog to handle AMS related complexities
- RF/Very high-speed designs (including SerDes) related verification challenges and tricks used in practice
- Testbench Acceleration techniques to meet modern ultra-complex chip verification challenges - case studies and experiences
- Functional Coverage closure techniques and its testbench design implications

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Submission Guidelines

Submit abstracts at DVCon-India.org beginning **March 1**.

To spare you the many hours of preparation associated with other paper submissions, DVCon India has the following process:

- Submit a 500-1000 word abstract highlighting what you wish to present at DVCon India. The program committee will evaluate your abstract. The deadline for abstract submission is **April 25, 2017**.
- Authors of exceptionally strong abstracts will be shortlisted for oral or poster presentation at the conference. They will present their work at DVCon India on September 14 or September 15.

An abstract is expected to include the following details:

1. A title
2. Name, affiliation, phone number and email addresses for all authors.
3. An introduction that specifies the context and motivation of the submission.
4. A summary of the specific contributions of your work.
5. A summary that highlights results. To evaluate your contribution, you must specify some results.
6. References, if appropriate

Your abstract can be at most two pages (exclusive of Author(s)' details). You can format it in single or double column. Provide enough details so that the Technical Program Committee can evaluate the potential quality and interest of your possible presentation at DVCon India.

A one-paragraph summary will not fulfill this requirement. Please note that submitted abstracts can be edited until the submission deadline of April 25, 2017. Download the abstract submission template at DVCon-India.org/call-abstracts.

Process for Accepted Abstracts

Authors of accepted abstracts will be expected to do the following in accordance with Conference deadlines:

- Submit a confirmation form to confirm all paper and author details.
- Produce a full paper for the conference proceedings.
- Complete a copyright form.
- Submit presentation slides for online distribution to conference attendees.

View/download past conference proceedings: visit DVCon-India.org/conference/history.

Questions? Feel free to contact support@mpassociates.com for questions on the submission process.