CONFERENCE PROGRAM
25-26 SEPTEMBER 2019

DVCon-India.org

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INDIA

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TABLE OF CONTENTS

GENERAL CHAIR’S WELCOME ................................................................. 4
Conference Sponsor ............................................................................. 5
Conference Details ............................................................................... 6
DVCon India 2019 Committees .............................................................. 8
Keynote ............................................................................................... 11

WEDNESDAY AGENDA ........................................................................ 12
Wednesday Session Details ................................................................ 14

THURSDAY AGENDA ........................................................................... 22
Thursday Session Details .................................................................... 24

DVCON INDIA EXPO
Thank You to Our Sponsors................................................................. 33
Exhibitor Listing & Floorplan ............................................................... 34
Exhibitor Details .................................................................................. 36
I am pleased to welcome you all to the 5th edition of DVCon India event planned on September 25-26th 2019 at Radisson Blu Hotel, Bangalore. DVCon India conference serves as the largest technical platform where Design and Verification engineers meet, network and exchange new and innovate ideas on addressing today’s challenges and pave the way for future improvements in tools, flows and methodologies. Growing demand for highly skilled design and verification engineers in the Indian subcontinent, is driving the need for close collaboration between EDA vendors, Standards body and Product companies to equip the new workforce with the latest technologies and tools. Many emerging facets of design verification including Low Power/MSIP Design Verification, Static/Formal Verification, Safety Critical Design Verification, Machine Learning & Big Data, Portable Stimulus, ESL & Virtual Prototyping will be the focus of discussion in the form of Tutorials, panel discussions, technical presentation and keynote speeches. The Steering committee comprising of highly experienced and seasoned design & verification experts from various semiconductor companies have spent significant effort in tailoring the agenda for the two days to address various needs of the engineers and make it a great learning and sharing experience. I am very eagerly looking forward to seeing all of you at the conference, actively participate and make the event a grand success!!

Sanjay Muchini

DVCon India 2019 General Chair
Accellera Systems Initiative, the proud sponsor of DVCon India 2019, is an independent organization with the mission to provide design and verification standards required by systems, semiconductor, IP and design tool companies to enhance a front-end design automation process. We collaborate with our community of companies, individuals and organizations in delivering the standards that lower the cost to design commercial EDA, IC and embedded system solutions. As a result of its partnership with the IEEE, Accellera standards are transferred to the IEEE Standards Association for formalization and ongoing change control.

**Accellera Systems Initiative: A New Synergy for Standards**

System, software, and semiconductor design are converging to meet the increasing challenges to create complex integrated circuits and system on chips. This convergence has brought to the forefront the need for a single organization to facilitate the creation of system-level, semiconductor design, and verification standards. Leading industry standards associations Accellera Organization Inc. and the Open SystemC Initiative (OSCI) merged in 2011 to form a single organization, Accellera Systems Initiative, to address the needs of the system and semiconductor designers who must find new and smarter ways to create and produce increasingly complex chips. The new organization will evolve to create more comprehensive standards that benefit the global electronic design community.

**Membership**

Accellera members directly influence development of the most important and widely used standards in electronic design. Member companies protect and leverage their investment in design languages through their funding of a proven, effective and responsible organization. In addition, our members have a higher level of visibility in the EDA industry as active participants in Accellera-sponsored activities and as contributors to its decisions, which impact the EDA industry. For a full list of technical activities that are supported by Accellera, and for information on how to join us, please visit our website at www.accellera.org.

**Accellera Global Sponsors**

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REGISTRATION HOURS
Location: Closed Registration Area
Wednesday, 25 September --- 08:00 - 18:30
Thursday, 26 September------- 08:00 - 18:30

EXPO HOURS
Location: Closed Pre Function Area
Wednesday, 25 September --- 11:00 - 18:30
Thursday, 26 September------- 11:00 - 17:30

TUTORIALS & PROCEEDINGS DISTRIBUTION
DVCon India Conference Papers and Tutorial presenter slides will be delivered electronically online via a username and password.
To access: http://proceedings.dvcon-india.org
Username: proceedings@dvconindia.org
Password: 519838w
TEA BREAKS & NETWORKING RECEPTION

Enjoy a tea break while you mingle with DVCon India’s exhibitors, located in hallway outside of the technical session rooms, conference area.

**Wednesday, 25 September**
- 11:00 - 11:30 | Location: Closed Pre Function Area
- 15:30 - 16:00 | Location: Closed Pre Function Area
- 17:30 - 18:30 | Location: Closed Pre Function Area

**Thursday, 26 September**
- 11:00 - 11:30 | Location: Closed Pre Function Area
- 15:30 - 16:00 | Location: Closed Pre Function Area
- 17:30 - 18:30 | Location: Grand Victoria Ballroom

SOCIAL MEDIA AT DVCON INDIA

Follow @DVConIndia on Twitter and tweet about your experience and highlights at the conference!
Don’t miss DVCon on Facebook at Facebook.com/DVConIndia.

AWARDS PRESENTATION

**Thursday, 26 September, 17:30 - 18:30 | Location: Grand Victoria Ballroom**

Join us to close the conference with an awards ceremony, featuring the 2019 Best Paper and Best Poster award winners and more!
2019 COMMITTEES

TECHNICAL PROGRAM COMMITTEE

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KEYNOTES

WEDNESDAY, 25 SEPTEMBER

KEYNOTE: THE EVOLUTION OF STATIC VERIFICATION
Sridhar Seshadri - Synopsys, Inc.
09:45 - 10:30 | Grand Victoria Ballroom

KEYNOTE: DRIVING DIGITALIZATION WITH A BOUNDARY FREE INNOVATION PLATFORM
Stefan Jockusch - Siemens PLM Software Inc.
11:30 - 12:15 | Grand Victoria Ballroom

THURSDAY, 26 SEPTEMBER

INVITED KEYNOTE: MODEL FOR PRODUCT DEVELOPMENT TO TARGET BEST IN CLASS TTM WITH SINGLE STEPPING QUALITY
Anil Kempanna - Intel Corp.
09:45 - 10:30 | Grand Victoria Ballroom

EXHIBITS & NETWORKING RECEPTION

Enjoy networking with other DVCon India attendees while visiting the many interesting exhibitors located in hallway outside of the technical session rooms, conference area.
Opening Talks & Lamp Lighting Ceremony | Room: Grand Victoria Ballroom

Keynote: The Evolution of Static Verification | Sridhar Seshadri

Panel: Can Designs be Signed Off with Formal Verification Alone? | Room: Grand Victoria Ballroom

Tea Break and Exhibits Networking | Room: Closed Pre Function Area

Keynote: Driving Digitalization With A Boundary Free Innovation Platform | Room: Grand Victoria Ballroom

Panel: AI/ML in Design and Verification - Problems/Solutions, Challenges

Lunch Break | Room: Closed Lawn

Short Workshop: Effective Verification of RISC-V Cores and SoCs | Room: Arabica

Tutorial: System Level Flows for SoC Architecture Analysis and Design | Room: Robusta

Tutorial: Simulation Acceleration to speed block and platform level IP verification | Room: Grand Victoria Ballroom

Short Workshop: System Level Flows for SoC Architecture Analysis and Design | Room: Robusta

Tutorial: Next Generation System Design and Verification for Transportation | Room: Grand Victoria A

Short Workshop: Leveraging Virtual Realization to make Portable Stimulus UVM/SDV Scenarios Portable | Room: Arabica

Tutorial: Using Verification Continuum Platform to Speed PCIe System Verification | Room: Robusta

Short Workshop: Applying Design Patterns to Maximize Verification Reuse @Block, Subsystem and System-on-Chip Level | Room: Arabica

Exhibits and Networking Reception | Room: Closed Pre Function Area
**WEDNESDAY’S AGENDA**

**Ballroom**

<table>
<thead>
<tr>
<th>Room: Grand Victoria Ballroom</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Tutorial: Simulation Acceleration to speed block and platform level IP verification</strong></td>
</tr>
<tr>
<td>Room: Grand Victoria A</td>
</tr>
<tr>
<td><strong>Tutorial: PSS: From (a Brilliant) Idea to a Winning Formula</strong></td>
</tr>
<tr>
<td>Room: Grand Victoria B</td>
</tr>
<tr>
<td><strong>Panel: Can Designs be Signed Off with Formal Verification Alone?</strong></td>
</tr>
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</tr>
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</tr>
<tr>
<td>Sridhar Seshadri</td>
</tr>
<tr>
<td>Room: Grand Victoria Ballroom</td>
</tr>
<tr>
<td><strong>Opening Talks &amp; Lamp Lighting Ceremony</strong></td>
</tr>
<tr>
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<tr>
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</tr>
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</tr>
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</tr>
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</tr>
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</tr>
<tr>
<td>Room: Grand Victoria A</td>
</tr>
<tr>
<td><strong>Tutorial: Modern SystemC</strong></td>
</tr>
<tr>
<td>Room: Grand Victoria B</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Room: Closed Pre Function Area</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Tea Break and Exhibits Networking</strong></td>
</tr>
<tr>
<td>Room: Closed Pre Function Area</td>
</tr>
<tr>
<td><strong>Keynote: Driving Digitalization With A Boundary Free Innovation Platform</strong></td>
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<tr>
<td>Stefan Jockuschi</td>
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<td>Room: Grand Victoria Ballroom</td>
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<td>Room: Grand Victoria Ballroom</td>
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**Technologies and Solutions**

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Opening Talks and Lamp Lighting Ceremony  
**Time:** 09:30 - 09:45 | **Room:** Grand Victoria Ballroom  
Join us for the opening session of the 2019 Design and Verification Conference and Exhibition India, featuring the lamp lighting ceremony.

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**Keynote: The Evolution of Static Verification**  
**Time:** 09:45 - 10:30 | **Room:** Grand Victoria Ballroom  

Static verification aims to find RTL bugs efficiently. It has evolved from Lint to CDC and RDC, to cover all aspects of design. As design complexity has increased, so has the number of clocks, resets and power domains. What was once considered a large full-chip five years ago is now an IP; one of 50 blocks in a large SoC. This keynote looks at the static verification landscape and how it has evolved to support chip complexity, along with the unique challenges and opportunities posed by sophisticated chips for automotive systems, AR/VR platforms, and AI applications with 5G connectivity. Can machine learning help designers be productive and mitigate growing SoC challenges?

**Biography:** Sridhar Seshadri, Vice President R&D in the Verification Group at Synopsys, is responsible for static verification solutions. He received his bachelor’s degree in computer science from Bangalore University and master’s degree from SUNY Buffalo. Sridhar has over 25 years of EDA experience. Highlights from various roles at Synopsys include lead on VCS simulator team for performance optimizations and driver of SystemVerilog implementation in VCS, delivery of VC Static Platform, VC LP and VC Formal, and management of ZeBu R&D with an emphasis on unique solutions in emulation debug.

**Speaker:**  
Sridhar Seshadri - Synopsys, Inc.

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**Panel: Can Designs be Signed Off with Formal Verification Alone?**  
**Time:** 10:30 - 11:15 | **Room:** Grand Victoria Ballroom  

Formal verification has improved in leaps and bounds in recent years, in performance, capacity and usability. Once only effective for control-dominated designs with shallow state-space, formal is nowadays being applied to much more complex designs involving data transportation and even data transformation, with increasing complexity and state depth. But are we at the point where complex designs can be signed off with formal alone? At what point is simulation still required?

**Takeaways:** The panel audience should hear lively debate with useful advice on the following:  
- Formal verification metrics and sign-off methodology  
- Where simulation is still necessary  
- How UVM-based and formal verification are used together in practice  
- Best practices for combining formal and simulation coverage for metric-driven sign-off

**Panelists:**  
- Ramana Venkata Barala - Qualcomm Research  
- Sudhakar Surendran - Texas Instruments  
- M. V. A. Kiran Kumar - Intel Corp.  
- Pete Hardee - Cadence Design Systems, Inc.

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**Thank you to our Sponsor**
Tea Break & Networking
Time: 11:15 - 11:30 | Room: Closed Pre Function Area
Enjoy a tea break while you mingle with DVCon India’s exhibitors, located in hallway outside of the technical session rooms, conference area.

Keynote: Driving Digitalization With A Boundary Free Innovation Platform
Time: 11:30 - 12:15 I Room: Grand Victoria Ballroom
We are witnessing a radical change of the way products are created, produced, and utilized. As a consequence of continuing digitalization, leading technology companies are pursuing the idea of a complete, high fidelity “digital twin” that makes the boundaries between the design process of mechanical parts, electronics, embedded software, sensors and specialized IC and sensor technology are disappearing.

This digital twin is becoming a necessity. Autonomous driving, as an example, puts an end to the feasibility of verifying the functionality of today’s and tomorrow’s vehicles through road testing. A complete virtualization of mechanical properties, physics, electronics, real-time software, down to the sensor data processing at the IC level is the only avenue to verify the safety and functionality of advanced driver assistance systems and autonomous functions. In the same way, technologies like additive manufacturing, advanced materials and exploding variation require an extensive virtualization of the production process to accelerate verification.

Biography: Dr. Stefan Jockusch is vice president of Strategy for Siemens Digital Industries Software, a business unit of Siemens Digital Industries. Dr. Jockusch drives strategic business planning and market intelligence as well as coordinates business activities across all business segments and with Digital Industries leadership. Dr. Jockusch has served in a number of business leadership and R&D management roles, driving the development and market introduction of radically innovative mechatronic systems. Prior to his current assignment, Dr. Jockusch was vice president of Automotive Industry Strategy, leading the company’s business development and portfolio planning efforts for the automotive industry. He began his career at Siemens as a management consultant with Siemens Corporate Technology. He later moved to Siemens AG as executive board assistant for the industry, transportation and technology sectors, where he led several strategic initiatives. A U.S. and German citizen with broad international experience, he relocated to the United States in 2001 and later decided to make the U.S. his family’s permanent home. Stefan holds a PhD summa cum laude in natural sciences from University of Bielefeld and a master’s degree in physics from the University of Göttingen.

Speaker: Stefan Jockusch - Siemens PLM Software Inc.

Panel: AI/ML in Design and Verification - Problems/Solutions, Challenges and Effectiveness
Time: 12:15 - 13:00 I Room: Grand Victoria Ballroom
Moderator: Sidhartha Mohanty - Intel Corp.
Panelists: Badri Gopalan - Synopsys, Inc.
Ruchir Dixit - Mentor, A Siemens Business
Hrishikesh Sathyavasu Murukkathampoondi - Arm, Ltd.
Lunch Break
Time: 13:00 - 14:00 | Room: Closed Lawn

Take time to network and mingle with other conference attendees while enjoying a buffet lunch. Exhibits will be open throughout the conference area, so be sure to stop by the booths and see what’s new.

Short Workshop: Effective Verification of RISC-V Cores and SoCs
Time: 14:00 - 14:45 | Room: Arabica

Organizer:
Tom Anderson - OneSpin Solutions GmbH

RISC-V is changing the game for IP providers and SoC designers. Providers can offer commercial cores without the need to acquire expensive licenses, while open-source implementations are already available. SoC teams that want to use RISC-V processors have many choices, with even more options expected soon. The sheer number of companies and products using RISC-V guarantees a rich ecosystem and a good chance of industry disruption.

However, design integrity is a challenge for both core developers and core integrators. To be successful, IP vendors must compete against long-established processor families with decades of proven silicon. RISC-V cores must be thoroughly verified as functionally correct to satisfy the Instruction Set Architecture (ISA) and other requirements. Integrators must be certain that cores are fully compliant, and many will want to re-verify the one they choose.

Hardware Trojans or other unintended logic can be inserted at multiple points in the development process. Showing that the RISC-V core can be trusted requires proving that no such issues exist. Only formal verification has the potential to prove both ISA compliance and trust. Some types of unintentional design errors can also provide an attack gateway. Analysis of both the RISC-V core and the SoC that integrates it can prove that the design is secure.

This workshop provides guidance for RISC-V core vendors who need to verify their IP, developers of cores for internal consumption, engineers evaluating cores for possible use, and SoC teams integrating RISC-V cores from internal or external sources. The workshop agenda is as follows:

- Challenges for RISC-V verification
- Formal specification of the ISA
- Formal verification of ISA compliance
- Detection of Trojans and malicious logic
- Detection of hardware security holes
- Examples from verification of open-source cores
- Examples from verification of open-source SoCs
- Future work and summary

Speaker:
Nicolae Tusinschi - OneSpin Solutions GmbH

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Tutorial: System Level Flows for SoC Architecture Analysis and Design

Time: 14:00 - 15:30 | Room: Robusta

Organizer:
Umesh Sisodia - CircuitSutra Technologies Pvt. Ltd.

A Case Study of Single Source Methodology for Early SoC Development

The complexity of SoC design is increasing everyday in terms of number of gates, architecture etc. Along with the increasing complexity, today’s designs have to be efficient in terms of power/performance/area. If we follow the traditional approach of design development, then meeting the above requirements within the demanding time-to-market constraints will be very challenging.

In current design development methods, design and architecture issues are identified much later in the design cycle leading to ECO (Electronic Change Order), thus affecting time to market. In this section, we will discuss multiple system level methodologies @Infineon which enables early design analysis, facilitating ‘Shift Left’. The ‘Shift Left’ approach has been introduced to domains like power intent/estimation, timing constraints checks and floor planning, thus assisting SoC architects to do ‘what-if’ analysis and make correct decisions much early in the design cycle. This approach is also extended to embedded software domain for enabling customers to develop early application software using Virtual Prototypes.

Defining a SystemC Methodology for your Company

As SystemC gains popularity in the fields of architecture evaluation, virtual platform development, SoC level verification etc, more teams and companies want to explore, experiment and deploy it for their modeling usecases. While SystemC library provides the vocabulary and the nuts and bolts to build a useful and diverse set of models, it is sometimes too low level to be immediately useful. What is needed is a SystemC library analogous to Boost libraries in C++, for building blocks like memories, buses, registers, timers etc along with the infrastructure to quickly stitch them together into a working platform asap. Most of the Semiconductor companies who have successfully deployed SystemC, have developed their own tool independent methodology on top of SystemC, and they use it together with advanced modeling tools from EDA vendors. Such a library usually starts with basic building blocks, and over a period of time becomes a very rich collection of re-usable modeling components that can be re-used across various IP models, SoC variants, Modeling Use cases, Business units etc.

Any company looking to adopt SystemC in their flows should carefully conceptualize development of such a methodology inhouse, and can learn from the best practices being followed in the Industry. In this presentation we will talk about what should be the content of such a methodology/library and how it should be conceptualized.

CircuitSutra has worked with leading semiconductor companies for more than a decade now and has participated in modeling projects from the stage of experimentation to pilot projects and to widespread adoption. We have in-depth understanding of the best practices followed in the modeling domain.

Using High-Level Synthesis to migrate Software Algorithms to Semiconductor Chip designs

High-Level Synthesis (HLS) raises the abstraction of chip design beyond RTL. It enables implementation of design functionality in high level languages like C++/SystemC, and generates corresponding RTL using the HLS tools. Synthesizable C++/SystemC code for a design is very concise compared to resulting RTL code for the same design, and simulation of C++/SystemC models is much faster compared to RTL simulation. This allows significant productivity gains in design and verification process. HLS also allows separation of functionality from architecture constraints and technology parameters, thus permitting code re-use across different variants of semiconductor chips, or across FPGA and ASICs.

HLS flows are more effective for algorithm centric designs. Nowadays we see new chip design requirements for emerging domains like 5G, Deep Learning, Vision, Image Processing, Speech, Audio processing etc. In these domains there are many algorithms implemented in software, and several of these are available as open source.

In this talk we will present a HLS based methodology to quickly migrate a software algorithm implemented in C/C++ to a hardware implementation in RTL for semiconductor chips (FPGA orASIC). We will also cover a verification flow that allows use of the original testsuite of the software algorithm to verify the synthesizable C++/SystemC model as well as the final RTL. The untimed C++/SystemC models are also suitable to be used in Virtual Platforms, that allows embedded software development much before the chip is designed.

This methodology accelerates the pace of innovation, enables faster roll out of new chips, permits experimentation by quickly trying out the functionality in software and hardware, and taking high level architecture decision much earlier in the cycle.

Speakers:
Ajay Goyal - Infineon Technologies
Swaminathan Ramachandran - CircuitSutra Technologies Pvt. Ltd.
Umesh Sisodia - CircuitSutra Technologies Pvt. Ltd.

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**Tutorial: Simulation Acceleration to Speed Block and Platform Level IP Verification**

**Time:** 14:00 - 15:30  |  **Room:** Grand Victoria A

**Organizer:**
Prashanth Srinivasa - Synopsys, Inc.

Simulation Acceleration effectively addresses the runtime performance challenges of a simulation platform, by providing up to 100X speedup over simulation. This enables users to not only find bugs quicker, but also achieve a “shift left” through performance analysis and power estimation much earlier in the design cycle.

User friendly features, acceleration VIPs and debug are key requirements for a seamless integration and quicker adoption of simulation acceleration technology.

This tutorial discusses the new simulation acceleration technology with Synopsys VCS® and ZeBu®, with a focus on:
- Reusing SystemVerilog/UVM testbenches to move from simulation to acceleration step by step
- Ways of finding performance bottlenecks through profiling and guidelines to improve the performance
- Debug features and effective ways of debugging a verification environment

**Speakers:**
- Prashanth Srinivasa - Synopsys, Inc.
- Rajesh Kumar Meda - Synopsys, Inc.

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**Tutorial: PSS: From (a Brilliant) Idea to a Winning Formula**

**Time:** 14:00 - 15:30  |  **Room:** Grand Victoria B

**Organizer:**
Sharon Rosenberg - Cadence Design Systems, Inc.

The Portable Stimulus and testing Standard (PSS) represents a revolution in users’ ability to express IP and system functional dependencies to fuel a new generation of tools. Assuming prior exposure to PSS by most of the audience, this technical tutorial spends minimal amount of time on PSS concepts using a real-life application and a demo. Most of the session is devoted to practical aspects of PSS adoption:
- What value should I get from PSS on my first project, and what benefits are expected in subsequent projects?
- Does it make sense to use coverage and Metric Driven Verification (MDV) with PSS?
- How should PSS users capture regressions?
- How exactly is coreless-to-core reuse achieved?
- What are the options in handling register programming?

The tutorial is targeted for technical leads and managers that are doing HW verification (with or without UVM) or C test-writers creating SW tests in bare-metal or on top of an operating system. While the tutorial is technical and can benefit experienced PSS users, no previous PSS knowledge is needed for beginners.

**Speaker Biography:** Sharon Rosenberg is a senior architect at Cadence. Sharon received his B.A. in computer science from Bar-Ilan University and joined Verisity Design in 1996 to lead the hardware testbench automation revolution. Sharon introduced many of the most used UVM concepts, including agents, factory, configuration mechanism, and sequences as the technical leader of the Cadence UVM team. Sharon represented Cadence in the Accellera UVM working group and co-authored the book A Practical Guide to Adopting the Universal Verification Methodology. Currently, Sharon is driving portable stimulus solution technology for SoC verification and represents Cadence in the Accellera Portable testing and Stimulus (PSS) Working Group.

**Speaker:**
Sharon Rosenberg - Cadence Design Systems, Inc.
Short Workshop: Shift-Left Verification of Digital and Mixed-Signal Designs using MATLAB

Time: 14:45 - 15:30 | Room: Arabica

Organizer:
Vidya Viswananthan - MathWorks, Inc.

Speakers:
Aniruddha Dayalu - MathWorks, Inc.
Sunita John - MathWorks, Inc.

Tea Break & Networking
Time: 15:30 - 16:00 | Room: Grand Victoria Foyer

Enjoy a tea break while you mingle with DVCon India’s exhibitors, located in hallway outside of the technical session rooms, conference area.

Tutorial: Using Verification Continuum Platform to Speed PCIe System Verification
Time: 16:00 - 17:30 | Room: Robusta

Organizer:
Anunay Bajaj - Synopsys, Inc.

PCIe as a high speed and high throughput bus is used more and more frequently, especially for high-performance computing, AI, and 5G applications. PCIe verification is complex as requirements stem from many levels:

• Application layer with verification and system performance analysis of applications, drivers and algorithms
• Transaction layer
• Data link layer for PCIe controller

Full system design, including the PHY layer and PCS and SERDES verification

In this workshop, we will introduce 3 typical solutions: PCIe verification IP (VIP) for System/PCS/SERDES verification, virtual host PCIe solution with ZeBu emulator, and prototyping solution for system validation with HAPS, that enable chip designers to meet the power, performance and area requirements and “shift-left” PCIe verification.

Short Workshop: Leveraging Virtual Realization to Make Portable Stimulus UVM/SDV Scenarios Portable
Time: 16:00 - 16:45 | Room: Arabica

Organizer:
Dave Kelf - Breker Verification Systems, Inc.

The current Accellera Portable Stimulus Standard requires a fair amount of user coding to allow scenarios to be ported between UVM and Software Driven Verification (SDV) SoC flows. Exec blocks must be written with low level SystemVerilog and C Test code. The committee is looking at ways to improve this, and layers already exist that allow for UVM Sequence generation, Hardware Software Interfacing (HSI), and more. This tutorial will show how a Virtualization layer eliminates a lot of low level coding, accelerating both UVM and SDV test generation, and allowing PSS generated test content to be easily loaded into existing test benches.

Speaker:
Dave Kelf - Breker Verification Systems, Inc.
Tutorial: Next Gen System Design and Verification for Transportation

Time: 16:00 - 17:30 | Room: Grand Victoria A

Organizer:
Rebecca Granquist - Mentor, A Siemens Business

Increased intelligence and autonomy of next-generation transportation products are driving the ICs behind those moving machines to become some of the most advanced semiconductor products in the industry. As a result, this is disrupting how you design, verify and develop these ICs.

Starting with design, the entrance of machine learning using neural networks and inference solutions has demonstrated the need to quickly develop these highly algorithmic designs. Validation of those algorithms, performance targets, and power consumption demands new solutions that can simulate the complex, heterogeneous systems with real world interactions. Beyond just ensuring the IC operates correctly, functional safety standards, like ISO 26262 for automotive, are enforcing state-of-the-art practices, strict processes and evidence for compliance to ensure the delivered capabilities are functionally safely. The days of separating functional workflow development from the safety workflow has passed. It is imperative that safety be at the forefront when determining the methodologies and tools to deploy in the creation of your transportation application.

The intersection of these challenges is delivering advanced features on-time, within budget all while simultaneously ensuring the IC will not malfunction.

This tutorial we will demonstrate how to use these next-generation IC development practices to build and validate smarter, safer ICs. Specifically, it will look at:

- How to use High-Level Synthesis (HLS) to accelerate the design of smarter IC’s
- How to use emulation to provide a digital twin validation platform beyond just the IC
- How to use develop functionally safe IC’s

Target Audience: Design and Verification Engineers and Managers

Speakers:
- Pradeep Salla - Mentor, A Siemens Business
- Richard Pugh - Mentor, A Siemens Business
- Ellie Burns - Mentor, A Siemens Business
- Sandeep Dager - Mentor, A Siemens Business

Tutorial: Modern SystemC

Time: 16:00 - 17:30 | Room: Grand Victoria B

Organizer:
David Long - Doulos

Much of the code found in today’s SystemC applications is based on the 1998 or 2003 versions of C++. The C++ language has changed considerably since then, with major additions added from 2011 onwards. Future versions of the SystemC standard will depend on language features added in C++11 and C++14 (“modern C++”): the current SystemC CCI standard already does! This tutorial will highlight significant C++11 and C++14 changes and show how they can be used to create improved, “modern SystemC” code.

Speaker Biography: Dr David Long is the Principal Member of Technical Staff at Doulos, where he has worked since 2001, developing and presenting training courses and providing consultancy services. During that time he has trained several thousand engineers in more than 20 different countries, in subjects ranging from HDL-based design and verification of digital and mixed-signal hardware through to virtual prototypes and embedded software. He is an expert in hardware description languages such as SystemVerilog, SystemC and VHDL and verification methodologies such as UVM. He is an active member of several Accellera Systems Initiative working groups and is the co-author of the IEEE 1666 SystemC Language Reference Manual. Prior to joining Doulos, he worked for over 15 years in both industry and academia. He has an MSc in VLSI Design and a PhD in Mixed-Signal Simulation.

Speaker:
David Long - Doulos
Short Workshop: Applying Design Patterns to Maximize Verification Reuse @Block, Subsystem and System-on-Chip Level

**Time: 16:45 - 17:30 | Room: Arabica**

**Organizer:**
Paul Kaunds - Sondrel Ltd

In this tutorial, we will provide an in-depth analysis of various planning, implementation, debug and coverage closure challenges faced in functional verification at block level, subsystem and system-on-chip level. By taking relevant examples we will demonstrate how these issues can be either avoided or solved by applying Design Patterns mainly Environment, Stimulus and Analysis Patterns. We will also highlight some of the benefits like configuration and re-usability of UVM and C code.

**Speakers:**
- Revati Bothe - Sondrel Ltd
- Kiran Kodakandla - Sondrel Ltd
- Manish Singhal - Sondrel Ltd

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Exhibits & Networking Reception

**Time: 17:30 - 18:30 | Room: Grand Victoria Foyer**

Enjoy networking with other DVCon India attendees while visiting the many interesting exhibitors, located in hallway outside of the technical session rooms, conference area.

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<table>
<thead>
<tr>
<th>Time</th>
<th>Event</th>
<th>Room</th>
</tr>
</thead>
<tbody>
<tr>
<td>09:30 - 09:45</td>
<td>Opening Talks</td>
<td>Room: Grand Ballroom</td>
</tr>
<tr>
<td>09:45 - 10:30</td>
<td><strong>INVITED KEYNOTE: Model for Product Development to Target Best</strong></td>
<td>Room: Grand Victoria Ballroom</td>
</tr>
<tr>
<td>10:30 - 11:00</td>
<td>Poster Session</td>
<td>Room: Exhibit Area Corridor</td>
</tr>
<tr>
<td>11:00 - 11:30</td>
<td>Tea Break and Exhibits Networking</td>
<td>Room: Closed Pre Function Area</td>
</tr>
<tr>
<td>11:30 - 13:00</td>
<td><strong>Regular Session: Formal Verification</strong></td>
<td>Room: Robusta</td>
</tr>
<tr>
<td></td>
<td><strong>Regular Session: Design</strong></td>
<td>Room: Arabica</td>
</tr>
<tr>
<td>13:00 - 14:00</td>
<td>Lunch Break</td>
<td>Room: Closed Lawn</td>
</tr>
<tr>
<td>14:00 - 15:30</td>
<td><strong>Regular Session: Formal Verification</strong></td>
<td>Room: Robusta</td>
</tr>
<tr>
<td></td>
<td><strong>Regular Session: Analog</strong></td>
<td>Room: Arabica</td>
</tr>
<tr>
<td>15:30 - 16:00</td>
<td>Tea Break and Networking</td>
<td>Room: Closed Pre Function Area</td>
</tr>
<tr>
<td>16:00 - 17:30</td>
<td><strong>Regular Session: CDC</strong></td>
<td>Room: Robusta</td>
</tr>
<tr>
<td></td>
<td><strong>Regular Session: Machine Learning &amp; Automation</strong></td>
<td>Room: Arabica</td>
</tr>
<tr>
<td>17:30 - 18:30</td>
<td>Closing Ceremony and Awards</td>
<td>Room: Grand Victoria Ballroom</td>
</tr>
</tbody>
</table>
THURSDAY'S AGENDA

Best in Class TTM with Singler Stepping Quality | Anil Kempanna

Regular Session: Design & Functional Safety
Room: Arabica

Regular Session: UVM
Room: Grand Victoria A

Regular Session: ESL & Virtual Prototyping
Room: Grand Victoria B

Regular Session: Analog/AMS
Room: Arabica

Regular Session: MISC-I
Room: Grand Victoria A

Regular Session: Portable Stimulus
Room: Grand Victoria B

Regular Session: Machine Learning & Automation
Room: Arabica

Regular Session: MISC-II
Room: Grand Victoria A

Regular Session: Low Power
Room: Grand Victoria B

INVITED KEYNOTE: Model for Product Development to Target Best in Class TTM with Single Stepping Quality
Anil Kempanna
Room: Grand Victoria Ballroom

Poster Session
Room: Exhibit Area Corridor
Opening Talks
Time: 09:30 - 09:45 | Room: Grand Victoria Ballroom

Join us as we re-open the conference on Thursday with an opening talk from the Vice Chair. Look forward to an interesting schedule of keynotes, posters, and the technical paper sessions.

Tea Break & Networking
Time: 11:00 - 11:30 | Room: Closed Pre Function Area

Enjoy a tea break while you mingle with DVCon India’s exhibitors, located in hallway outside of the technical session rooms, conference area.

Invited Keynote: Model for Product Development to Target Best in Class TTM with Single Stepping Quality
Time: 9:45 - 10:30 | Grand Victoria Ballroom

In an environment of ever increasing design complexity of innovative products and reduced time-to-market, it is extremely critical to have first time right silicon. An engineering team needs to think through all aspects of product development from silicon-to-platform-to-software-to-customer and find ways to left shift product readiness. Key note walks through gaps, challenges and best practices for integrated solutions within and across product portfolios.

Biography: Anil Kempanna: Vice President, IoTG-HSPE, Silicon & IP. Anil leads the SoC-Horizontal team in HPG and also drives key SOC methodology improvements for Intel. In less than 3 years, Anil has built a strong 1000 member org in HPG to deliver 15+ SOCs with multiple innovations across domains. Anil has been instrumental in surfacing problem statements and driving solutions across teams World-Wide for many programs which has significantly reduced Time-To-Market. Anil is extremely passionate about grooming young leaders and fostering a culture of Quality, Predictability and Vibrancy across the teams he leads.

Anil has 25+ years of experience in the semiconductor industry in US, Europe and Asia. During his career, Anil has delivered over 40+ products in multiple market segments like Smartphones, Modems, IoT, Networking and Small Cell devices. Prior to joining Intel, Anil has worked in Qualcomm, Texas Instruments, Cadence and at a fixed Broadband wireless startup, Ensemble Communications.

Anil holds a Master’s degree in Science and Electrical Engineering from Wright State University and a Master’s degree in Business Administration from University of Phoenixautomotive industry. He began his career at Siemens as a management consultant with Siemens Corporate Technology. He later moved to Siemens AG as executive board assistant for the industry, transportation and technology sectors, where he led several strategic initiatives. A U.S. and German citizen with broad international experience, he relocated to the United States in 2001 and later decided to make the U.S. his family’s permanent home. Stefan holds a PhD summa cum laude in natural sciences from University of Bielefeld and a master’s degree in physics from the University of Göttingen.

Speaker: Anil Kempanna - Intel Corp
Poster Session
Time: 10:30 - 11:00 | Room: Closed Pre Function Area

13.1 Automatically Synthesizing Higher Level of Protocol Abstraction for Faster Debug and Deeper Insight into Modern Digital Designs
Amar Patel, Yogesh Badaya, Alasdair Ferro, Christopher Jones - Mentor Graphics

13.2 SoC Verification Enablement using HM Model
Vineet Tanwar, Chirag Kedia, Rahul Gupta - Qualcomm India Private Limited

13.3 First Test to Full Compliance
Anadi Shukla, Abhishek Yadav, Hemlata Bist, Manoj Kumar - Cadence Design Systems, India Pvt. Ltd.

13.4 Use of Message Bus Interface to Verify Lane Margining in PCIe
Ankita Vashist - Synopsys India Pvt Ltd

13.5 Building and Modelling Reset Aware Testbench for IP Functional Verification
Naishal Shah - Intel, Corp

13.6 Improving Simulation Performance at Subsystem/SoC Level using LITE ENV
Avni Patel, Heena Mankad - Intel, Corp

13.7 Verification Strategies and Modelling for the Uninvited Guest in the System: Clock Jitter
Deepak Nagaria, Vikas Makhija, Apoorva Mathur - Synopsys India Pvt. Ltd.

13.8 Adaptive UVM <-> AMOD Testbench for Configurable DSI IP
Krishnapal Singh, Pavan Yeluri, Ranjith Nair - NVIDIA, Corp.

13.9 Spec Automated Formal Verification of a Security Module with a Hybrid of Formal Property and Security Path Verification Tools
Karthik Rajakumar - Texas Instruments

13.10 From Device Trees to Virtual Prototypes
Sakshi Arora, Vikrant Kamboj, Preeti Sharma - Synopsys India Pvt. Ltd.

13.11 Enabling SystemC/TLM-2.0 Compliant Virtual Prototypes with Fault Injection Capability
Chethan Nayak, Nikhil Jain - Infineon Technologies India Pvt. Ltd

13.12 High Level Synthesis to Bridge the FPGA to ASIC Gap
Anoop Saha - Mentor A Siemens Business

13.13 Break the SoC with Random UVM Instruction Driver
Pravin Wilfred, Madhukar Mahadevappa, Bogdan Todea, Diana Dranga - Microchip Technology, Inc.

13.14 Systematic Asynchronous FIFO Verification using Structural Analysis and Formal Techniques

Session 1 - Formal Verification
Time: 11:30 - 13:00 | Room: Robusta

Chair:
Girish Marudwar - Synopsys, Inc.

Formal Verification (FV) technology and methodology has come long way and has become main stay along with simulations. With advent of multiple apps, we see many engineering teams have adopted formal verification and achieved shift left in their verification cycles. In pursuit of shifting left further, experts are innovating new ways to apply FV to non-conventional problems. In this first session on Formal Verification these innovations will show you that there is lot of potential in FV technology which is still out there to be unearthed and get benefited

1.1 Step-Up Your Register Access Verification
Nisha Kadhirvelu, Sundar Krishnakumar - Cypress Semiconductor Technology India Pvt Ltd
Rimpy Chugh - Mentor Graphics (India) Pvt. Ltd.
Wesley Park - Mentor, A Siemens Business

1.2 Bringing DataPath Formal to Designers’ Footsteps
Achutha Kiran Kumar V. Madhunapantula - Intel Corp.
Disha Puri, Shriya Dharade - Intel, Corp

1.3 Formal for Adjacencies: Expanding the Scope of Formal Verification
Achutha Kiran Kumar V. Madhunapantula, Bindumadhava S. Singanamalli - Intel Corp.
Vichal Verma, Savitha Manojna - Intel Technology India Pvt. Ltd
Session 2 - Design & Functional Safety

**Time:** 11:30 - 13:00 | **Room:** Arabica

**Chair:**
Pankaj Singh - Cadence Design Systems, Inc.

While the tools and methodology for ISO 26262 functional safety verification of digital design has matured, the overall effort is complex and time consuming especially for higher level of ASIL compliance requirements. Traditional approach is to rely on simulation based safety verification.

Formal tools can be utilized not only for systematic faults but also for random fault verification. This session has innovative presentations which provides holistic hybrid approach towards achieving desired functional safety verification goals by using simulation and formal approach in an efficient manner. Besides safety verification this session also describes challenges involved in design of response tracking system that is necessary in SoC with complex IP interaction requiring protocol conversion.

2.1 High Frequency Response Tracking System Micro-Architecture

Sateesh Vadlamuri, Gopalakrishnan Sridhar - Intel, Corp

2.2 Formal Assisted Fault Campaign for ISO26262 Certification

Nitin Ahuja, Sandeep Jana - Synopsys India Pvt. Ltd.
Mayank Agarwal - NXP Semiconductors

2.3 Assisting Fault Injection Simulations for Functional Safety Signoff using Formal

Pulicharla Ravindrareddy - Analog Devices, Inc.

Session 3 - UVM

**Time:** 11:30 - 13:00 | **Room:** Grand Victoria A

**Chair:**
Amit Agarwal - NVIDIA Corp.

UVM has become first choice for verification engineers across the VLSI industry, to create testbenches and for verifying IP’s & sub-systems. This session will provide an insight into some of the application of UVM like implementing UVM RAL coverage using prediction logic, enhancement in the inbuilt UVM Reg model to provide additional capabilities for register/memory verification. This session will also provide a deep dive of UVM based testbench to verify LDPC (Low Density Parity Checker) Codec design. At the end of session, UVM users will get to learn about the improvements that other teams are doing over and above the existing capabilities of inbuilt UVM library and will also learn how UVM can be used effectively to achieve coverage driven verification closure.

3.1 Enhanced LDPC Codec Verification in UVM

Anand Shirahatti, Shriharsha Koila, Ganesh Shetti - VerifSudha Technologies Pvt Ltd
Prateek Jain - Yoctozant Technologies Pvt. Ltd.

3.2 Leveraging UVM IEEE 1800.2 for Improved RAL Modelling

Vikas Sharma, Manoj Manu, Ankit Garg - Mentor, A Siemens Business

3.3 Functional-Coverage Sampling in UVM RAL: Use of 2 Obscure Methods

Muneeb Ulla Shariff - Mirafræ Technologies
Ravi Reddy - Roche Sequencing
Session 4 - ESL & Virtual Prototyping
Time: 11:30 - 13:00 | Room: Grand Victoria B

Chair:
Swaminathan Ramachandran - CircuitSutra Technologies Pvt. Ltd.

Virtual Platforms have become ubiquitous, no longer is the question whether to use them, nor how to build them, not even how to use them; today the focus is on the next big performance gains. We will see three different approaches: novel new technology, approaches to optimising models, and big leaps forward in abstractions. As applications and system complexity continues to increase, these novel techniques are all required for us to stay ahead and allow Virtual Platforms to continue to be the cornerstone of system development.

4.1 Open Source Virtual Platforms for SW Prototyping on FPGA Based HW
Chen Qian, NVIDIA Corp.
Mark Burton - GreenSocs Ltd
Praveen Wadikar - NVIDIA Corp.

Amit Dudeja, Amit Tara, Amit Garg, Tushar Jain - Synopsys India Pvt. Ltd.

4.3 Profiling Virtual Prototypes: Simulation Performance Analysis & Optimization
Sandeep Jain - NXP Semiconductors

Lunch Break
Time: 13:00 - 14:00 | Room: Closed Lawn

Take time to network and mingle with other conference attendees while enjoying a buffet lunch. Exhibits will be open in hallway outside of the technical session rooms, conference area.

Session 5 - Formal Verification
Time: 14:00 - 15:30 | Room: Robusta

Chair:
Girish Marudwar - Synopsys, Inc.

In this session we want to raise the bar further from first sessions on Formal Verification (FV) technology and methodology. Now a days we are no more worried about coverage numbers but are looking for finding more bugs. The presenters in this session will talk about advance techniques deployed beyond the normal use models and making formal more effective and efficient. There are unique new challenges which are discussed and innovative solutions are presented with case studies and results. These methodologies can be readily picked and applied on your challenging designs.

5.1 Formal Verification of Low-Power RISC-V Processors
Ashish Darbari - Axiomise Ltd.

5.2 Simulation Guided Formal Verification with “River Fishing” Techniques
Bathri Narayanan Subramanian, Ping Yeung - Mentor, A Siemens Business

5.3 Challenges of Formal Verification on Deep Learning Hardware Accelerator
Satish Yellinidi Dasarathanaidu - Intel, Corp
Session 6 - Analog/AMS

Time: 14:00 - 15:30 | Room: Arabica

Chair:
Sriram K S - Samsung Research & Development Institute India - Bangalore

AMS DV enables the engineers of analog and mixed signal systems and integrated circuits to create/model continuous time and event driven models for verification of complex analog, mixed signal circuits. From being used/implemented in isolated pockets, the AMS is gaining momentum at exponential pace and will be an inevitable part of DV closure/sign-off. The complex techniques used in bringing the two unique worlds of Digital and Analog together is not just challenging but time consuming as well.

6.1 Simulation Analog Fault Injection Flow for Mixed-Signal Designs
Pablo Cholbi, Dylan O'Connor Desmond, Raman K - Analog Devices, Inc.

6.2 Challenges, Complexities and Advanced Verification Techniques in Stress Testing of Elastic Buffer in High Speed SERDES IPs
Kamesh Velmail, Suvadeep Bose, Parag Lonkar, Somasunder Sreenath - Samsung Electronics Co., Ltd.

6.3 DV Methodology to Model Scalable/Reusable Component to Handle IO Delays/Noise/Crosstalk in Multilane DDR PHY IF
Tapas Ranjan Jena, Gaurav Kumar, Gowdra Bomanna Chethan, Sriram Kazhiyur Sounderrajan, Somasunder Kattepura Sreenath - Samsung Semiconductor India R&D, Bangalore

Session 7 - MISC-I

Time: 14:00 - 15:30 | Room: Grand Victoria A

Chair:
Karthikeyan Subramanian - Qualcomm India Pvt. Ltd.

In this session of papers on verification infrastructure, portability and validation, you will uncover and learn about Design Patterns, these are foundations of UVM. Once the testbench infrastructure is in place, you will see how using Python one can create portable tests for both in Pre-Silicon and Post-Silicon and finally you will see how one can achieve validation of Firmware in pre-silicon simulation and also getting coverage on Firmware code.

7.1 Using Software Design Patterns in Test Bench Development for a Multi-Layer Protocol
Pavan Yeluri - NVIDIA, Corp
Ranjith Nair - NVIDIA, Corp

7.2 Unified Test Writing Framework for Pre and Post Silicon Verification
Rahulkumar Patel, Pablo Cholbi, Sivasubrahmanya Evani, Raman K - Analog Devices, Inc.

7.3 Towards Early Calibration of Firmware using UVM Simulation Framework
Amaresh Chellapilla, Pandithurai Sangaiyah - Intel, Corp
Session 8 - Portable Stimulus
Time: 14:00 - 15:30 | Room: Grand Victoria B

Chair:
Ramana Barala - Qualcomm India Pvt. Ltd.

Accellera’s emerging Portable Test and Stimulus Standard (PSS) defines a specification to create a single representation of stimulus and test scenarios usable by a variety of users across many levels of integration under different configurations. In this exciting track we will see how various companies adopt PSS which defines high-level verification intent and creates test cases targeting different execution environments, such as simulation, emulation, hardware prototypes, and real silicon. Here we will see some of the limitations of this upcoming standards and how different teams use techniques blended with tool support to overcome these challenges. Overall this session will benefit new users, who are trying to adopt this for legacy SV/UVM/C test framework reuse and give insight in to preserving existing tests and enable portability across blocks to SoC test benches.

8.1 Designing A PSS Reuse Strategy
Matthew Ballance - Mentor, A Siemens Business

8.2 Benefits of PSS coverage at SOC and its Limitations
Sundararajan Haran, Saleem Khan - Qualcomm India Pvt. Ltd.

8.3 A Pragmatic Approach Leveraging Portable Stimulus from Subsystem to SOC Level and SOC Emulation.
Joachim Geishauser, Karandeep Singh, Aditya Chopra, Nitin Verma - NXP Semiconductors

Tea Break & Networking
Time: 15:30 - 16:00 | Room: Grand Victoria Foyer

Enjoy a tea break while you mingle with DVCon India’s exhibitors, located in hallway outside of the technical session rooms, conference area.

Session 9 - CDC
Time: 16:00 - 17:30 | Room: Robusta

Chair:
Manu Chopra - Cadence Design Systems, India Pvt. Ltd.

Modern low power designs are logically split into multiple clock domains, power domains and reset domains. In this session we discuss some of the experiences and challenges faced with clock and reset domains - with methodology recommendations for effective verification.

9.1 Exhaustive Reset Verification Enablement: A PCIE Reset Verification Case study
Rohit K. Sinha, Praveen Dornala - Intel Technology India Pvt. Ltd

9.2 Our Experience of Glitches at Clock Trees, Reset Trees and CDC Paths
Jebin Mohandas - Intel, Corp

9.3 Scalable Multi-Domain Multi-Variant Reset Management in Complex Verification IPs
Kaustubh Kumar, Munnangi Sirisha, Lokesh Kumar - SiliConch Systems
Session 10 - Machine Learning & Automation
Time: 16:00 - 17:30 | Room: Arabica

Chair: Prasanna Keshavan - HCL Technologies Limited

Automation in the VLSI project cycle provides the advantages of improving productivity and quality while reducing errors and adding flexibility to the process. In this session we have a couple of papers that talk about the automation implemented in the design flow that helped in efficiency improvement. The rise of machine learning (ML) has introduced many opportunities for computer-aided-design, VLSI design, and their intersection. We have an interesting submission that talks about a scalable and parameterized HW architecture that can be used to build a convolutional and fully connected neural network used in ML applications.

10.1 Hardware Implementation of Smallscale Parameterized Neural Network Inference Engine
Vishnu Bharadwaj, Shruti Narake - Manipal Institute of Technology
Saurabh Patil - Intel, Corp

10.2 Automatic Generation of Infineon Microcontroller Product Configurations
Leily Zafari, Boyko Traykov, Prateek Chandra - Infineon Technologies

10.3 Automation of Waiver and Design Collateral Generation for Scalable IPs
Gopalakrishnan Sridhar, Sateesh Vadlamuri, Midhun Krishna - Intel, Corp

Session 11 - MISC-II
Time: 16:00 - 17:30 | Room: Grand Victoria A

Chair: Pradeep Salla - Mentor Graphics (India) Pvt. Ltd.

In this “potpourri” session of papers on miscellaneous topics, verification (process) automation is the keen common thread that rings throughout to improve consistency, quality and ultimately verification productivity. One paper vows to simplify functional coverage implementation through automated generation of a complete package of SystemVerilog coverage models that can be readily connected to your UVM testbench. A second paper similarly focuses on accelerating functional coverage closure using a novel method for writing goal-oriented tests with smart stimulus constraint models that ensure coverage goals are reached with certainty and without redundancy. A third paper proposes an automated approach for easier, scalable integration of verification IP and testbench components into an SoC platform.

11.1 Uncover: Functional Coverage Made Easy
Akash S, Rahul Jain, Gaurav Agarwal - NVIDIA Corp.

11.2 Architecturally Scalable Testbench for Complex SoC
Senthilnath Subbarayan, Arulanandan Jacob - Qualcomm India Pvt. Ltd.

11.3 Goal Driven Stimulus Solution - Get Yourself out of the Redundancy Trap
Rohit Bansal - Samsung Electronics Co., Ltd.
Session 12 - Low Power

Time: 16:00 - 17:30 | Room: Grand Victoria B

Chair:
Ashok Natarajan - Intel Corp.

Low power design is a necessity today in all SOC’s. With the declining gate length in new process technologies, power dissipation has become a much bigger problem than what it was few years ago. As companies started packing more and more features and applications on the battery operated devices, battery backup time became very important. Nowadays, power is replacing performance as a key competitive metric and an increasingly important criterion from the customers. In this session we have some interesting Low power design/verification techniques employed by some leading technology teams that helped solve this challenge.

12.1 Simplifying Hierarchical Low Power Designs using Power Models in Intel Design
Rohit K. Sinha - Intel Technology India Pvt. Ltd

12.2 Low Power Techniques in Emulation
Pragati Mishra, Jitendra Aggarwal - Arm, Ltd.

12.3 Low Power Validation on Emulation Using Portable Stimulus Standard
Deepinder Mohoora, Joydeep Maitra, Vikash Kumar Singh - Intel Technology India Pvt. Ltd

Closing Ceremony and Awards

Time: 17:30 - 18:30 | Room: Grand Victoria Ballroom

Join us to close the conference with an awards ceremony, featuring the Best Paper and Best Poster award winners and more.
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SYNOPSYS
**Exhibit Hours:**

Wednesday, 25 September --- 11:00 - 18:30  
Thursday, 26 September ----- 11:00 - 17:30

--- **DVCON INDIA 2019 EXHIBITORS** ---

Agnisys, Inc. ...................................... 9  
Avery Design Systems, Inc. ............ 16  
Breker Verification Systems, Inc.... 13  
Cadence Design Systems (India) Pvt. Ltd................................. 11

--- **EXHIBITOR FLOOR PLAN** ---

As of 26 August 2019
<table>
<thead>
<tr>
<th>Company</th>
<th>Booth</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mentor, A Siemens Business</td>
<td>15</td>
</tr>
<tr>
<td>Mirabilis Design Inc.</td>
<td>10</td>
</tr>
<tr>
<td>Mirafra Software Technologies Pvt Ltd.</td>
<td>2</td>
</tr>
<tr>
<td>PRO DESIGN Electronic GmbH</td>
<td>8</td>
</tr>
<tr>
<td>Real Intent, Inc.</td>
<td>7</td>
</tr>
<tr>
<td>SmartDV Technologies India</td>
<td>12</td>
</tr>
<tr>
<td>Sondrel Ltd.</td>
<td>21</td>
</tr>
<tr>
<td>Synopsys, Inc.</td>
<td>4</td>
</tr>
<tr>
<td>Truechip Solutions Pvt. Ltd.</td>
<td>3</td>
</tr>
</tbody>
</table>
Agnisys, Inc.

Booth: 9
www.agnisys.com

Agnisys Inc. is the leading supplier of Electronic Design Automation (EDA) software for solving complex design and verification problems for system development. Its products provide a common specification-driven development flow to describe registers and sequences for system-on-chip (SoC) and intellectual property (IP) enabling faster design, verification.

Avery Design Systems, Inc.

Booth: 16
www.avery-design.com

A leader in Verification IP providing robust models, compliance test suites, and services for PCI Express, USB/xHCI, UFS/FSHCl, NVMe/f, SATA Express, SATA, UniPro, Soundwire, Sensewire, CSI/DSCI, HDMI, DP, eMMC, SDIO, DDR4/LPDDR4, HBM, HMC, OENI/TOGGLE, CAN FD, LIN, FlexRay, and ACE/AKX/AKX/AH. A leader in verification tools. SimXACT automatically eliminates X bugs in RTL and gate-level simulation. ResetOPT minimizes reset/retention design overhead.

Breker Verification Systems, Inc.

Booth: 13
www.brekersystems.com

Breker uses a single, comprehensible, executable intent specification based on enhanced Portable Stimulus, for easy and fast scenario modeling. An AI-driven test synthesizer converts abstract scenario models into rigorous portable test sets that rapidly detect complex bugs. Breker’s unique deployment models allow the tests to be loaded into existing UVM & SoC environments with zero modification.

Cadence Design Systems (India) Pvt. Ltd.

Booth: 11
www.cadence.com

Cadence enables electronic systems and semiconductor companies to create innovative end products that are transforming our lives. Cadence software, hardware and semiconductor IP are used by customers to get to market faster. The company’s Intelligent System Design™ strategy helps customers develop differentiated products—from chips to boards to intelligent systems—in mobile, consumer, automotive, aerospace, IoT, industrial and other markets. www.cadence.com

CircuitSutra Technologies Pvt. Ltd.

Booth: 6
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CircuitSutra is an Electronics System Level (ESL) design IP and services company, headquartered in India, having development centers in Noida and Bangalore, and serves the customers worldwide. It enables customers to adopt advanced methodologies based on C, C++, SystemC, TLM, IP-XACT, UVM-SystemC, Portable Stimulus. Its core competencies include Virtual Prototype (Development, Verification, Deployment), Architecture & Performance modeling, High Level Synthesis, SoC & System verification.

Coverify

Booth: 20
www.coverify.com

Coverify is an Indian startup focussing on verification tools and services. Our opensource product, Embedded UVM (or EUVM) is the only port of IEEE 1.0 UVM that enables highly parallelized testbenches on multicore processors. EUVM compiles natively to embedded platforms, thus enabling hardware-software co-verification, and native testbenching on SoC/FPGA emulation platforms.

Doulos

Booth: 14
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Doulos has set the industry standard for high quality training and KnowHow for 28 years in design and verification languages and methodologies for system, hardware, and embedded software designers. The essential choice for 3800+ companies across 70+ countries, Doulos provides scheduled classes across North America and Europe, and delivers on-site and live online training worldwide. Find out more: www.doulos.com

MathWorks India Pvt Ltd.

Booth: 17
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MathWorks is the leading developer of mathematical computing software. Engineers and scientists worldwide rely on its products to accelerate the pace of discovery, innovation, and development. MATLAB and Simulink are used throughout the automotive, aerospace, communications, electronics, and industrial automation industries as fundamental tools for research and development. They are also used for modeling and simulation in increasingly technical fields.

Mentor, A Siemens Business

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Mentor, a Siemens Business, has pioneered technology to close the design and verification gap to improve productivity, and quality of results. Catapult® High-Level Synthesis for C-level verification and PowerPro® for power analysis; Questor® for simulation, low-power, VIP, CDC, Formal, Portable Stimulus and Functional Safety; Velocor® for hardware emulation and system of systems verification, unified with the Visualizer® debug environment.
Mirabilis Design Inc.

Mirabilis Design provides Electronic System-Level software for architecture exploration of semiconductors. Using VisualSim, designers can measure the timing, throughput, power and functional correctness. VisualSim is a graphical modeling and batch simulation for rapid model construction using trace inputs, visualization, standards library and custom development environment. VisualSim detects system bottlenecks, reports corner cases and export test cases with expected output.

Mirafra Software Technologies Pvt Ltd.

Mirafra is a global leader in the niche field of customised semiconductor chip design and verification services, helping customers build their next generation products. Over the past 15+ years, Mirafra has worked with world’s top semiconductor companies, providing end-to-end product engineering services, from specification to silicon and has contributed to hundreds of successful product tape-outs.

PRO DESIGN Electronic GmbH

Company description: PRO DESIGN is a privately held company based in Germany. The company’s products and services include the proFPGA product family of ASIC Prototyping and FPGA systems. The proFPGA system is a complete, scalable and modular (multi-)FPGA solution, which fulfills highest needs in the area of FPGA based Prototyping.

Real Intent, Inc.

Real Intent provides intent-driven static signoff tools to accelerate early functional verification of digital designs, leading the industry in precision, performance, and capacity. Its product capabilities for eliminating complex design failure modes include: clock domain crossing sign off from RTL through gate level, including multimode CDC; reset domain crossing sign off; and advanced RTL linting and analysis.

SmartDV Technologies India

SmartDV Technologies is the Proven and Trusted choice for Verification Intellectual Property (VIP) and Design IP. With the largest portfolio in the industry, its VIP is compatible with verification languages, platforms and methodologies. Supporting simulation, emulation and formal verification, FPGA, formal models and post-silicon validation platforms tools used in a coverage-driven verification flow. Connect with SmartDV at: Twitter: @SmartDV.

Sondrel Ltd.

Sondrel is Europe’s largest independent SoC design consultancy providing complete semiconductor solutions from concept to packaged silicon and outsourced design services down to 7nm. Sondrel designs SoCs for some of the world’s leading technology companies and specialises in high definition video processing, AI, automotive functional safety and secure IoT design. Sondrel is a UK, privately owned business founded in 2002.

Synopsys, Inc.

Synopsys is the Silicon to Software partner for innovative companies developing electronic products and software applications. Synopsys Verification Continuum combines best-in-class technology, including simulation, verification IP, emulation, advanced debug, static and formal verification, prototyping and virtual prototyping, with advanced methodologies enabling users to address rapidly escalating SoC complexity, accelerate time-to-market and bring products to market sooner.

Truechip Solutions Pvt. Ltd.

Truechip, the Verification IP specialist, is a leading provider of design and verification solutions. Truechip’s portfolio of Verification IPs includes Ethernet, USB, PCIe, LPDDR, HMC, HBM, AMBA, MIPI etc. All of Truechip’s VIPs are natively developed in System Verilog/ UVM. They also provide 100% functional coverage and include assertions compatible with formal/dynamic simulations. For more details visit us at www.truechip.net.
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