DVCon India 2019

25 – 26 September, 2019 | Radisson Blu, Outer Ring Road, Bangalore

Submission Deadline: 17 May, 2019

The Design & Verification Conference & Exhibition is the premier conference on the application of languages, tools, methodologies and standards for the design and verification of electronic systems and integrated circuits. The focus of this highly technical conference is on the practical aspects of these technologies and their use in leading-edge projects to encourage attendees to adopt similar techniques to improve their own design and verification flows.

In addition to the specific topic areas suggested below, submissions may incorporate:

- Usage of Electronic Design Automation (EDA) tools such as simulation, emulation, formal verification, virtual prototyping and/or FPGA prototyping
- FPGA-based designs
- Usage of specialized design and verification languages such as SystemVerilog, SystemC, and e
- Assertions in SVA or PSL
- The use of general purpose and scripting languages such as C, C++, Perl, Python, Tcl and others
- Applications of the new Accellera Portable Stimulus Standard
- Applications of design patterns or other innovative language techniques
- The use of AMS languages
- Internet of Things applications

This call for abstracts solicits for papers and corresponding presentations that are highly technical and reflect real-life experiences and emerging trends in various domains. Submissions are encouraged in (but not restricted to) the following areas:

Topic Area 1: VERIFICATION AND VALIDATION

- Advanced methodologies and testbenches
- Verification processes, regressions and resource management
- Debug and analysis of complex designs
- Multi-language design and verification
- Hardware/Software co-design and co-verification of embedded systems
- Gate level simulation methodology
- Assertion based verification
- UVM based coverage verification

Topic Area 2: DESIGN AND VERIFICATION REUSE AND AUTOMATION

- Bridging verification and validation across multiple engines
- SoC and IP integration methods and tools
- Applications of the Accellera Portable Stimulus Standard
- Configuration management of IP and abstraction levels
- Interoperability of models and/or tools
- Bridging virtual prototyping, simulation, emulation and/or FPGA prototyping
- Efficient algorithms for Design & Verification Automation

Topic Area 3: SAFETY-CRITICAL DESIGN AND VERIFICATION

- Verification and DO-254 compliance
- Automotive ISO 26262 Design and Verification Challenges
- Medical or Industrial Verification Challenges
- Requirements-Driven Verification Methodologies
- IP protection and security

Topic Area 4: MACHINE LEARNING AND BIG DATA

- Automating the Optimization of Design & Verification Processes
- Coverage metrics and data analysis
- Performance modeling and/or analysis

Topic Area 5: MIXED-SIGNAL DESIGN & VERIFICATION

- Mixed-signal design & verification techniques
- Real-value modeling approaches
- Application of mixed-signal extensions for UVM

Topic Area 6: LOW-POWER DESIGN & VERIFICATION

- Low-power design and verification
- Power modeling, estimation and management

Topic Area 7: STATIC & FORMAL VERIFICATION

- Clock Domain Crossing design and verification
- Formal Verification techniques and methodology
- Applications of Static and Formal techniques

Topic Area 8: ESL & Virtual Prototyping

- High-level synthesis from ESL languages
- Usage of a higher level of abstraction, SystemC modelling etc.
- Virtual Prototyping

PAPER SUBMISSION PROCESS

Note: New Submission Guidelines for DVCon India 2019

An initial submission is required before the full paper. The submission should be between a **minimum of 600 words and a maximum of 1200 words** (approximately 2 pages, not including diagrams, figures or tables).

In general, please provide enough details so that the Technical Program Committee can evaluate the potential quality and interest of your proposed presentation at DVCon India.

The initial submission should include:

- **Title**: The paper title.
- **Contact information**: Name, affiliation, phone number and email address for all authors.
- **Short Abstract**: Outline that clearly states the context and motivation of your contribution, approx. 100 words.
- **Related Work**: Identify other work on which this submission will be built, and the novelty of the paper.
- **Application**: Clearly describe the technical contribution, reflecting real life experiences, and its industrial application.
- **(Preliminary) results**: Summarize the results. State how these differ from previous work or state-of-the-art on the same subject.
- **Conclusions:** Summarize the major conclusions and findings presented in the paper.

Accepted authors will be invited and agree to do the following:

- Submit the final version of the paper (max. 8 pages) after incorporating feedback from the TPC (TBD)
- Register for the conference
- Submit a copyright form
- All accepted authors agree to present an oral or poster presentation at the conference (25 - 26 September, 2019).

Please note: Consistent with the requirements for other DVCon India presentations, your presentation may contain your company logo only on the title slide, and should use the provided templates.

Please make your initial submission by **17 May, 2019**.

IMPORTANT DEADLINES

- 17 May, 2019: Deadline for initial submission
- 28 June, 2019: Accept/reject notification sent to all authors
- 18 July, 2019: Full paper due for review by TPC
- 3 September, 2019: Final paper due
- 25 – 26 September, 2019: Conference.

CONFERENCE SCHEDULE

25 September, 2019 — Tutorials and exhibition

26 September, 2019 — Technical paper sessions, poster session, exhibition

DVCon India honors the **Best Paper/Presentation** and **Best Poster submissions**. The awards will be selected by the attendees at DVCon India based on the quality of both the paper and the presentation.

More information on DVCon India can be found on www.dvcon-india.org