Conference Program at a Glance

Day 1: Thursday, 25 September, 2014

	Grand Victoria 1 & 2 D1M1
9:30 - 9:45	**DVCon India Introduction & Overview** Umesh Sisodia, General Chair, DVCon
9:45 - 10:30	**Keynote Speech** Wally Rhines, CEO, Mentor Graphics Title: Accelerating EDA Innovation Through SoC Design Methodology Convergence
10:30 - 11:00	**Invited Keynote** Mahesh Mehendale, CTO, MCU, Texas Instruments Title: Challenges in the design and verification of ultra-low power "more than Moore" systems
11:00 - 11:30	Tea Break & Networking

	Grand Victoria 1 D1M2-ESL	Grand Victoria 1 D1M2-DV
11:30 - 12:00	**Keynote Speech** Title: High Level Synthesis and Verification Speaker: NEC	**Accellera Tutorial** Title: An Overview of UPF - IEEE 1801 Speaker: Amit Srivastava, Mentor Graphics
12:00 - 12:30	**Invited Talk** Title: Virtual Prototypes in Automotive from a Tier1 Perspective: Use Cases, Requirements and Challenges Speaker: Martin Vaupel, Robert Bosch	**Invited Talk** Title: Journey of Verification Speaker: Gaurav Jalan, Smartplay
12:30 - 13:00	**Technical Talk** Title: Sneak Preview of UVM-SystemC Speaker: Anupam Bakshi, Agnisys	**Invited Talk** Title: Verification IPs - Trends and Aspirations Speaker: Vijayabhaskar Sankaranarayanan, Cypress
13:00 - 14:00	Lunch Break	

	ESL Tutorials		DV Tutorials	
	Grand Victoria 1	Robusta	Grand Victoria 2	Boulangerie
14:00 - 15:30	**D1A1.1-ESL** Tutorial: Power Aware Architecture Definition and Software Development using Virtual Prototypes Presenter: Amit Garg (Synopsys)	**D1A1.2-ESL** Tutorial: SystemC AMS based methodologies for the design and verification of heterogeneous systems Presenters: Karsten Einwich (Fraunhofer IIS), Amarnath Reddy (CircuitSutra), V S Phaneendra Paluri (CircuitSutra)	**D1A1.1-DV** Tutorial: SystemVerilog for Design Presenters: Saminathan Chockalingam, Deepa Anantharaman (HCL)	**D1A1.2-DV** Tutorial: Achieving Portable Stimulus with Graph-Based Verification Presenters: Pradeep Salla (Mentor Graphics), Adnan Hamid (Breker Verification Systems), Srinivasan Venkataraman (CVC)
15:30 - 16:00	Tea Break & Networking			

	ESL Tutorials		DV Tutorials	
	Grand Victoria 1	Robusta	Grand Victoria 2	Boulangerie
16:00 - 17:30	**D1A2.1-ESL** Tutorial: Virtual Prototyping Methodologies, Applications, and a Case Study in Embedded System Development for a Motor Control Application with Fault Injection Analysis Presenters: Jay Yantchev (ASTC), Swaminathan Ramachandran (CircuitSutra), Arrun Prabhakaran (CircuitSutra)	**D1A2.2-ESL** Tutorial: Low Power Design & Verification Using High-Level Synthesis Presenters: Sanjiv Narayan, Vikas Tyagi and Vishal Sinha (Calypto)	**D1A2.1-DV** Tutorial: SoC Verification Challenges Offer Opportunities to Take a New Look at Debug Presenters: Amit Sharma (Synopsys), Srinivasan Venkataraman (CVC)	**D1A2.2-DV** Tutorial: Easier UVM – Making Verification Methodology more Productive Presenters: John Ansley, David Long (Doulos)
17:30 - 19:30	**Networking Cocktail/Snacks Party** Exhibits Open			

Day 2: Friday, 26 September, 2014

	Grand Victoria 1 & 2 D2M1
9:30 - 9:40	**Opening Talk** Ajeetha Kumari, Vice Chair, DVCon India
9:40 - 9:50	**Accellera Overview** Dennis Brophy, Accellera
9:50 - 10:35	**Keynote Speech** Janick Bergeron, Verification Fellow, Synopsys Title: Where is the Next Level of Verification Productivity Coming from?
10:35 - 11:05	**Invited Keynote** Vishwas Vaidya, Assistance General Manager - Electronics, Tata Motors Title: Automotive Embedded Systems: Opportunities and Challenges
11:05 - 11:30	Tea Break & Networking

	ESL Sessions & Accellera Tutorials D2M2-ESL	DV Papers D2M2-DV		
	Grand Victoria 1	Grand Victoria 2	Boulangerie	Arabica
11:30 - 12:00	**Accellera Tutorial** Overview of IP-XACT IEEE1685-2014 Standard Speaker: Prashant Karandikar (Texas Instruments)	**EMULATION, HW ACCELERATION, PROTOTYPING** **D2M2.1-DV** Title: Using Simulation Acceleration to Achieve 100X Performance Improvement with UVM Based Testbenches Speakers: Venkateswara Rao Narla, Ranjith Kumar Kotikalapudi, Vikas Verma and Gautam Kumar (Avago Tech) Title: Low Power Emulation for Power Intensive Designs Speakers: Harpreet Kaur, Piyush Kumar Gupta, Mohit Jain and Jitendra Aggarwal (ST) Title: MDLL and Slave Delay Line performance analysis using novel delay modeling Speakers: Avinash Shambu, Abhijith Kashyap and Kalpesh Shah (Texas)	**UVM** **D2M2.2-DV** Title: Responding to TAT Improvement Challenge through Testbench Configurability and Re-use Speakers: Akhila M, Kartik Jain and Mukesh Bhartiya (Intel) Title: Global Broadcast with UVM Custom Phasing Speakers: Jeremy Ridgeway and Dolly Mehta (Avago Tech) Title: Configuration in UVM: The Missing Manual Speaker: Mark Glasser (Nvidia)	**SELECTED TOPICS** **D2M2.3-DV** Title: A Framework for Verification of Program Control Unit of VLIW Processors Speakers: Sharangdhar Honwadkar and Santhosh Billava (Saankhya) Title: An Automated Systematic CDC Verification Methodology based on SDC setup Speakers: Sulabh Kumar Khare and Ashish Hari (Mentor) Title: Simulation Based Pre-Silicon Characterization Speakers: Venkatseema Das, Saurabh Pandey, Arif Mohammed and Nishant Gurunath (Texas Instruments)
12:00 - 13:00	**Panel Discussion** Title: System Modeling Life-cycle Challenges and Avenues: From Pre-silicon to Post-silicon Moderator: Saurabh Tiwari, Intel Panelists: AG Raghunath, Synopsys Bishnupriya Bhattacharya, Cadence Jay Yantchev, ASTC Umesh Sisodia, CircuitSutra Pradeep Ramachandran, Intel Amit Nene, Texas Instruments			

	ESL Papers		DV Papers		
	Grand Victoria 1	Robusta	Grand Victoria 2	Boulangerie	Arabica
14:00 - 15:30	**D2A1.1-ESL** Title: Runtime Fault-Injection Tool for Executable SystemC Models Speakers: Bogdan-Andrei Tabacaru, Moomen Chaari, Wolfgang Ecker and Thomas Kruse (Infineon) Title: Virtual Hardware Setup for Automotive Software Testing Speaker: Karthikeyan Ramachnadran (Robert Bosch) Title: Rapid Virtual Prototype Model Development using UML and IP-XACT Speakers: Deepak Kurapati, Aravinda Thimmapuram (Intel)	**D2A1.2-ESL** Title: RTL Quality for TLM Models Speaker: Preeti Sharma (Synopsys) Title: Trace Based Simulation Infrastructure For DDR Controller Evaluation Speaker: Abhilash Nair, Amit Nene, Ritesh Sojitra, Prashant Karandikar and Prajakta Bhutada (Texas Instruments) Title: Utilizing SystemC/TLM for adapting block level verification environment for reuse at System Level and Embedded Environments Speaker: Wasiq Zia (Cadence)	**ABV FORMAL, CDC, X-CHECK** **D2A1.1-DV** Title: Choice is Yours: Either Struggle to Tame "X" in the Wilderness of Multimillion Gates and Nets, OR Take it for a Walk in the RTL Park Speakers: Nitin Kumar Jaiswal, Harsh Garg and Mayank Digvijay Bindal (Freescale) Title: Model Extraction for Designs Based on Switches for Formal Verification Speakers: Naman Jain and Amar Patel (Mentor) Title: Usecase VCD (ValueChangeDump) Based Power Signoff Methodology for the Automotive SoC Speakers: Raghavendra Dattatraya, Poornima Prahlada, Manikandan Panchapakesan	**UVM, IP-TO-SOC REUSE** **D2A1.2-DV** Title: Bring IP Verification Closure to SoC, Scalable Methods to Bridge the Gap between IP and SoC Verification Speakers: Gaurav Gupta, Tejbal Prasad, Rohit Goyal, Vipin Verma and Sachin Jain (Freescale) Title: Reusable UVM_REG Backdoor Automation Speakers: Balasubramanian G, Bob Blais and Allan Peeters (PMC-Sierra) Title: UVM Usage for Selective Dynamic re-Configuration of Complex Designs Speakers: Kunal Panchal and Pushkar Naik	**SELECTED TOPICS** **D2A1.3-DV** Title: Compliance and Requirements-driven Development Methodology for Realizing System on Chip Based Solutions Based on ISO26262 Functional Safety Standard for Road Vehicle Speaker: Haridas Vilakathara (NXP) Title: Efficient Methods for Analog Mixed Signal Verification: Interface Handling Methods, Trade-offs and Guidelines Speakers: Lakshmanan Balasubramanian, Bharath Kumar Poluri, Shoeb Siddiqui and Vijay Kumar Sankaran (Texas, IITM,Candence) Title: Expediting Verification of Critical SoC Components using Formal Methods Speakers: Maddipatla Shankar Naidu, Lakshman Easwaran and Nuni Srikanth (Ericcson & Mentor)
15:30 - 16:00	Tea Break & Networking				

	ESL Papers & Accellera Tutorial		DV Papers		
	Grand Victoria 1	Robusta	Grand Victoria 2	Boulangerie	Arabica
16:00 - 17:30	**D2A2.1-ESL** Title: Design Methodology for Highly Cycle Accurate SystemC Models with Better Performance Speaker: Simranjit Singh and Sameer Deshpande (Infineon) Title: Data Flow Based Memory IP Creation Infrastructure Speaker: Abhilash Nair, Praveen Buddireddy, Rashmi Venkatesh, Tor Jeremiassen and Prajakta Bhutada (Texas Instruments)	**D2A2.2-ESL** Accellera Tutorial: SystemC/TLM-2.0 Tutorial with Sample Use Cases of FT and AT Models Speaker: Aravinda Thimmapuram (Intel)	**UVM** **D2A2.1-DV** Title: Parameterized and Re-usable Jitter Model for Serial and Parallel Interfaces Speakers: Amlan Chakrabarti and Malathi Chikkanna (AMD) Title: UVM, VMM and Native SV: Enabling Full Random Verification at System Level Speaker: Ashok Chandran (Analog Devices) Title: Cross-Domain Datapath Validation Using Formal Proof Accelerators Speakers: Aarti Gupta, Bindumadhava S S, Achutha Kiran Kumar M V, Jun B Liu (Intel)	**LOW POWER, CDC** **D2A2.2-DV** Title: Retention Based Low Power DV Challenges in DDR Systems Speakers: Subhash Joshi, Sangaiyah Pandithurai and Siddesh Halavarthi Math Revana (Qualcomm) Title: Low Power Verification Challenges and Coverage Recipe to sign-off Power Aware Verification Speakers: Deepmala Sachan, Thameem Syed S, Venugopal Jennarapu and Raghavendra Prakash (Intel) Title: Power Aware CDC Analysis at RTL for Faster Design Verification Closure Speakers: Anindya Chakraborty, Naman Jain, Saumitra Goel (Mentor)	**AMS** **D2A2.3-DV** Title: Automated Correct-by-Construct Methodology for RTL Design and Analog Mixed-signal Test Bench Generation Enables Early Design Closure of Mixed-signal SoC Speakers: Lakshmanan Balasubramanian, Murugesh Prashanth Subramaniam, Atul Ramakant Lele and Ranjit Kumar Dash (Texas Instruments) Title: Functional Verification of CSI2 Rx-PHY using AMS Co-simulations Speaker: Ratheesh Mekkadan (AMD) Title: SERDES Rx CDR Verification using Jitter, Spread-spectrum Clocking (SSC) Stimulus Speakers: Somasunder Sreenath, Raghuram Kolipaka, Chirag Shah and Parag Lonkar (Cadence)

	Hallway	
	ESL Posters	DV Posters
16:00 - 17:30	Title: High Level Modelling Of Physical Layer Noise Parameters Using SystemC Presenters: Prem Kumar Lohani, Ranjani K, Ravi Shankar R, Sundaresan C, Chaitanya Cvs (Whizchip & Manipal Edu) Title: Performance Estimation of Multi-Processors Systems with Hybrid Approach Presenter: Smei Habib	Title: How to Reuse Sequences with UVM ML-Open Architecture Presenters: Hannes Froehlich (Cadence) Title: A New Epoch is Beginning: Are You Getting Ready to Step into UVM1.2? Presenters: Roman Wang, Uwe Simm Title: Performance Verification of a 6Gbps HSLink Receiver Including Equalization and Clock Data Recovery using Mixed Signal Simulations Presenters: Aashish Bhide, Abhishek Chowdhary, Alok Kaushik, Vivek Uppal Title: Mixed-level Verification Methodology for Power-up Verification of eSRAMs Presenters: Prakhar Raj Gupta, Deepak Singhal, Rakesh Shenoy Panemangalore, Kshitij Verma Title: Gate-level Simulations - Continuing Value in Functional Simulations Presenters: Ashok Chandran and Roy Vincent Title: Pre-Silicon Debug Automation using Signature Extraction and Data-mining Presenters: Kamalesh Vikramasimhan, Senthilkumar Narayanaswamy, Kaustubh Godbole, Deepak Sadasivam Title: Please! Can Someone Make UVM Easy to Use? Presenters: Raghu Ardeishar and Rich Edelman (Mentor) Title: Performance Verification of a 6Gbps HSLink Receiver Including Equalization and Clock Data Recovery using Mixed Signal Simulations Presenters: Aashish Bhide, Abhishek Chowdhary, Alok Kaushik, Vivek Uppal

	Grand Victoria 1
17:30 - 18:00	**Closing Ceremony** Best Paper Awards, Raffles, and Closing Talk