Functional Verification of CSI2 Rx-PHY using AMS Co-simulations

Ratheesh Mekkadan

Advanced Micro Devices, Inc.

accellera SYSTEMS INITIATIVE

AMD

2014 DESIGN AND VERIFICATION DVCON CONFERENCE AND EXHIBITION INDIA

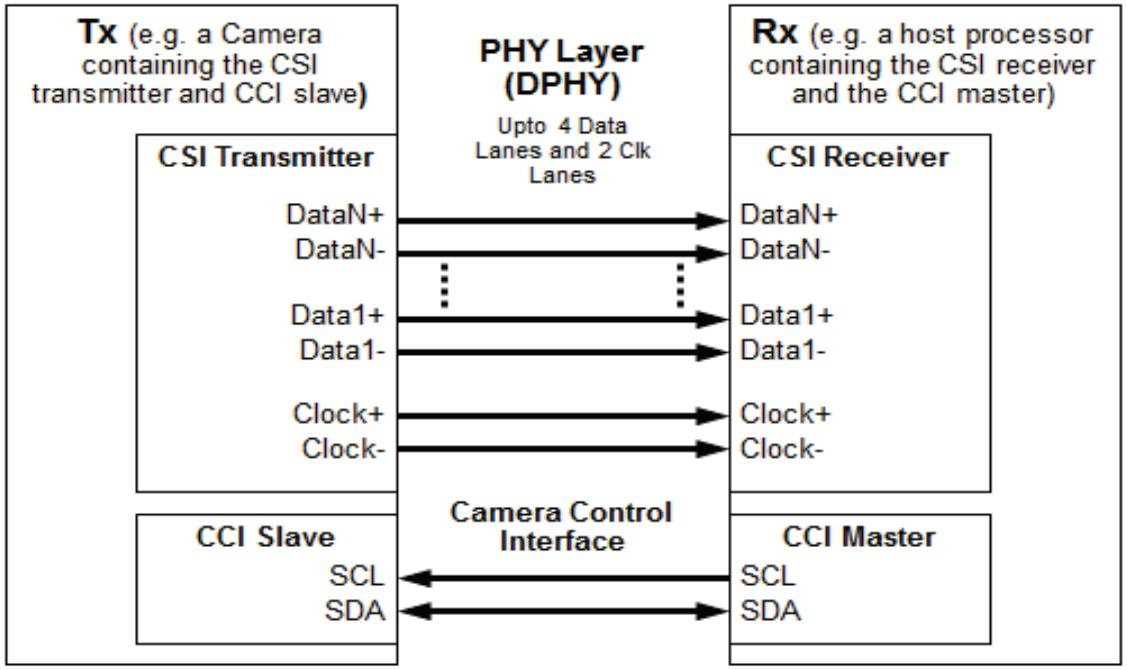
Agenda

- Introduction
- Scope of the Paper
- AMS Verification Approach
- Application and Results
- Conclusion
- Questions

Introduction

Introduction

- MIPI Camera Serial Interface 2 (CSI2) - standard interface between a peripheral device and host processor. Its Physical layer is the **MIPI DPHY**

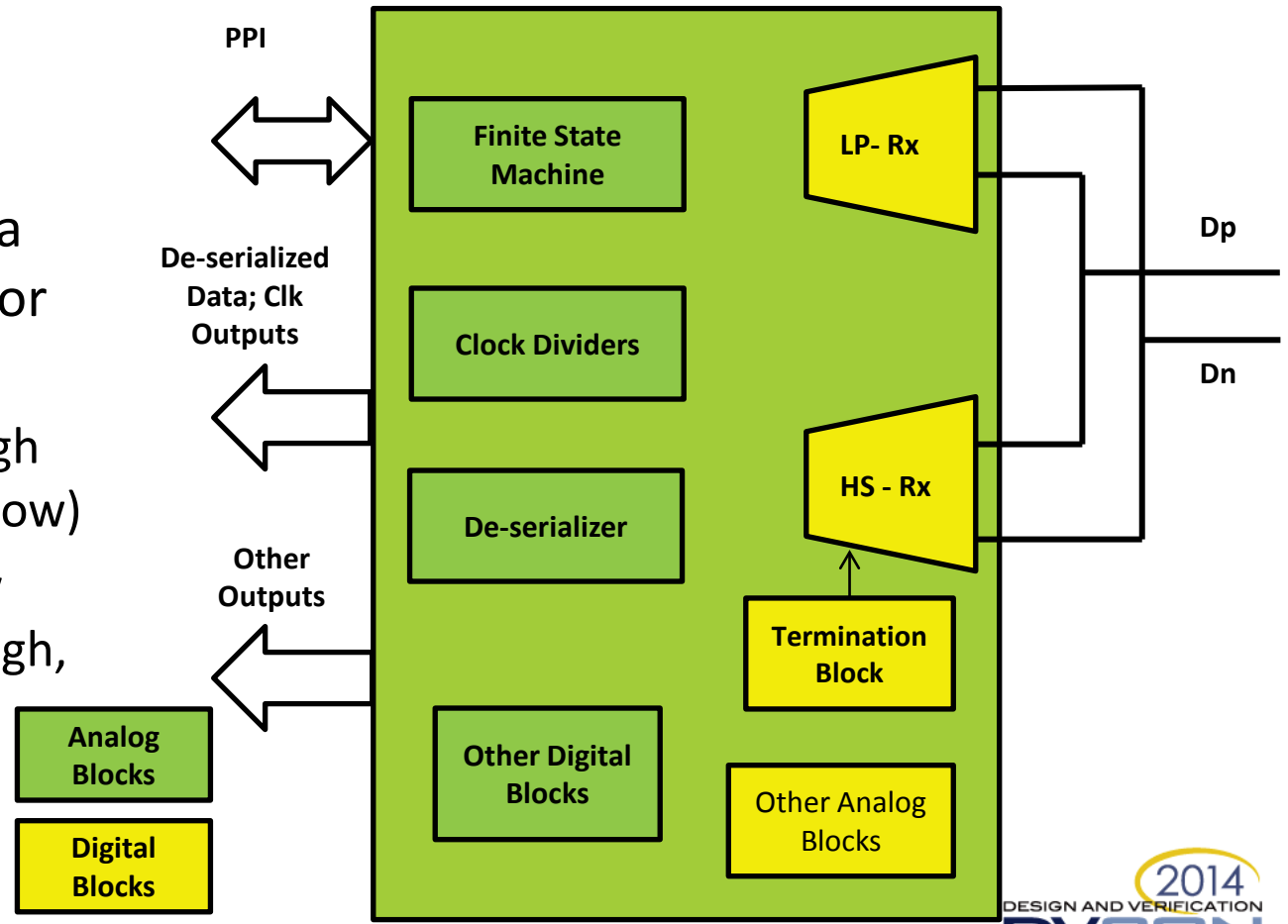


CSI2 PHY – An AMS IP

CSI2-PHY is an AMS IP

Supports HS mode data traffic and a LP mode for control sequencing

- LP -> Single Ended High Swing (1.2V high, 0V low)
- HS -> Differential Low Swing (e.g., 300mV high, 100mV low, 200mV common mode)



Operational Modes of CSI2 PHY

- DPHY **HS Mode** is used for data transfer in CSI2 protocol
- Data serialized in Tx PHY and de-serialized in Rx-PHY

- HS Mode sequencing seen for data transfer by Rx-PHY
  - LP-11 (StopState) ➔ LP-01(HS-Request) ➔ LP-00(HS- Prepare) ➔ HS-0 ➔[HS Sync Pattern -- HS Payload Data -- HS Trailer] ➔ LP-11 (StopState)
- During the HS Mode, the CSI2 PHY design enables line termination

Conventional RTL Verification Overview

- At IP/SoC simulations, RTL behavioral models are used for all analog blocks
- UVM based constrained random environment is used for verification.
  - Tb generates data bursts of random length and random data, error injection during start, payload or trail bits.
  - The UVM tb validates the mission mode and DFT functionality of the design.

Functional Verification Challenges

- RTL simulation environment is inadequate for verifying:
  - Functionality of the LP-Rx and the HS-Rx blocks
    - **LP and HS line voltage levels are different, but indistinguishable in a digital simulation.**
    - **Dynamic switching of voltages when transitioning LP <==> HS modes**
  - HS line termination
  - Analog functionality not modeled in the RTL behavioral model of the analog block

Scope of the Paper

Scope of the Paper

- Focus is on overcoming the challenges in conventional RTL verification of CSI2 Rx PHY

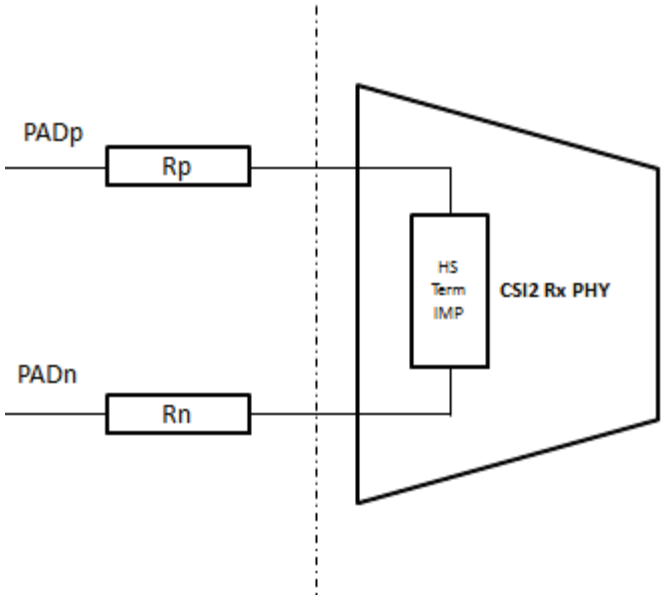
- The paper discusses:
  - How an Analog Mixed Signal (co-simulation) approach can be used
  - Additional scenarios can be covered using the cosim environment for functional verification of the CSI2 Rx PHY

AMS Verification Approach

AMS Verification Approach (1/3)

- Setup:
  - Top layer is the UVM testbench
  - Tool used: XA-VCS tool from Synopsys

- Key highlights of the setup:
  a) Analog and digital block partitioning for co-simulations
  b) Signal source impedance



AMS Verification Approach (2/3)

- Key highlights of the setup:

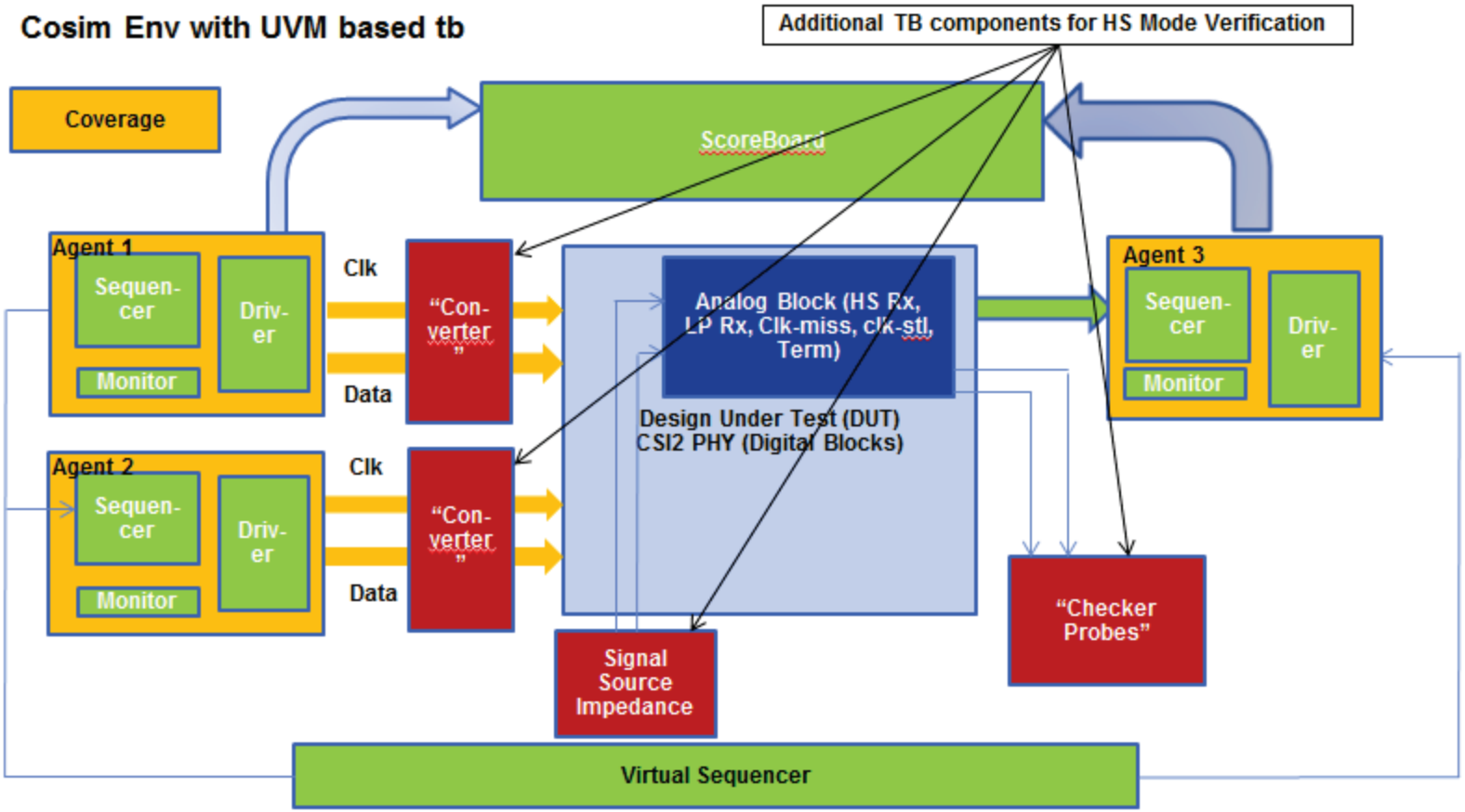
  c) Converter block - LP and HS line voltage levels are different, and dynamic switching of voltages occurs when transitioning LP <==> HS

  Normal d2a commands (from co-simulation tool) will not work here

Pseudo code:

```
always@(tb.hs_mode_en  or tb.pad_csi_dl_p) begin
      if(tb.hs_mode_en==1 && tb.pad_csi_dl_p==1)
         $snps_force_volt (<hierarchy>.PADPp, <hs_hi_voltage>);
      else if(tb.hs_mode_en==1 && tb.pad_csi_dl_p==0)
         $snps_force_volt (<hierarchy>.PADPp, <hs_low_voltage>);
      else if(tb.hs_mode_en==0 && tb.pad_csi_dl_p==1)
         $snps_force_volt (<hierarchy>.vpadp, <lp_hi_voltage>);
      else if(tb.hs_mode_en==0 && tb.pad_csi_dl_p==0)
         $snps_force_volt (<hierarchy>.vpadp, <lp_low_voltage>);
   end
```

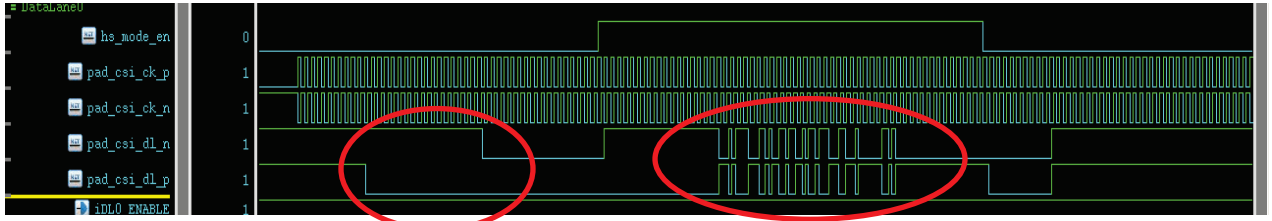
AMS Verification Approach (3/3)



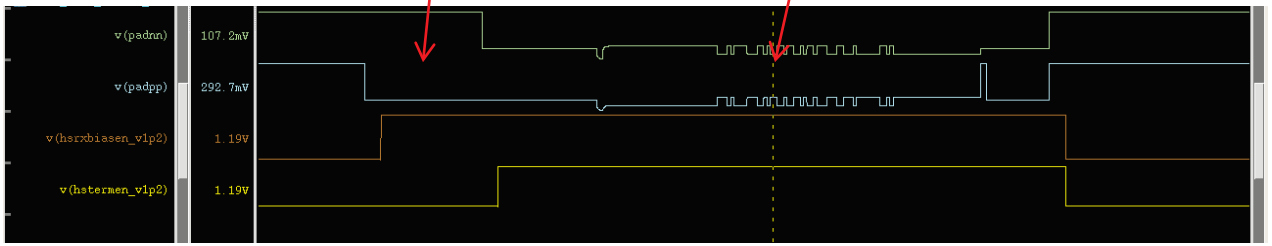
Application and Results

Application and Results (1/4)

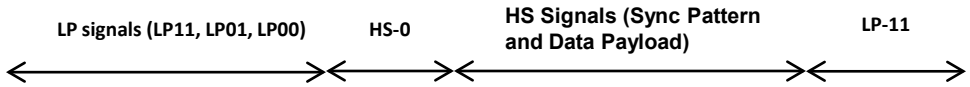
a) LP Rx and HS Rx functionality validated for “data transfer” mode (which uses LP to HS sequencing)

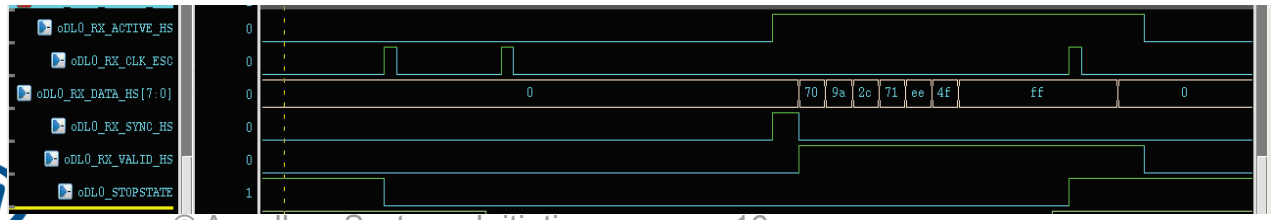


Stimulus from the Digital UVM testbench



Actual LP and HS voltage levels at the PADs





De-serialized data out of the CSI2 Rx-PHY

Application and Results (2/4)

b) Ensured valid voltage levels (per DPHY standard) are recognized by LP-Rx / HS-Rx by randomly varying voltage driven by “converter block”

Pseudo code

```
real  lp_hi_int_v, lp_hi_frac_v, lp_hi_v;
real  lp_low_int_v, lp_low_frac_v, lp_low_v;
lp_hi_int_v = $urandom_range(<LP_1_max>,<LP_1_min>);
lp_hi_frac_v = $urandom_range(999,1) / 1000;
lp_hi_v = lp_hi_int_v + lp_hi_frac_v;

lp_low_int_v = $urandom_range(<LP_0_max>,<LP_0_min>);
lp_low_frac_v = $urandom_range(999,1) / 1000;
lp_low_v = lp_low_int_v + lp_low_frac_v;
```

Application and Results (3/4)

c) CSR configuration of HS termination block

Pseudo code

a) Rx-PHY is powered-up and HS-Mode enabled

b) Fixed (HS differential level) voltages driven on PADs

c) Iterated through different settings for HS-termination

```
//thermometer coding; valid codes are 0,1,3,7,15,31,63,127
for (int i=0; i<8; i++) begin
   Term_CSR[6:0]={ Term_CSR [5:0], 1'b1};
end
```

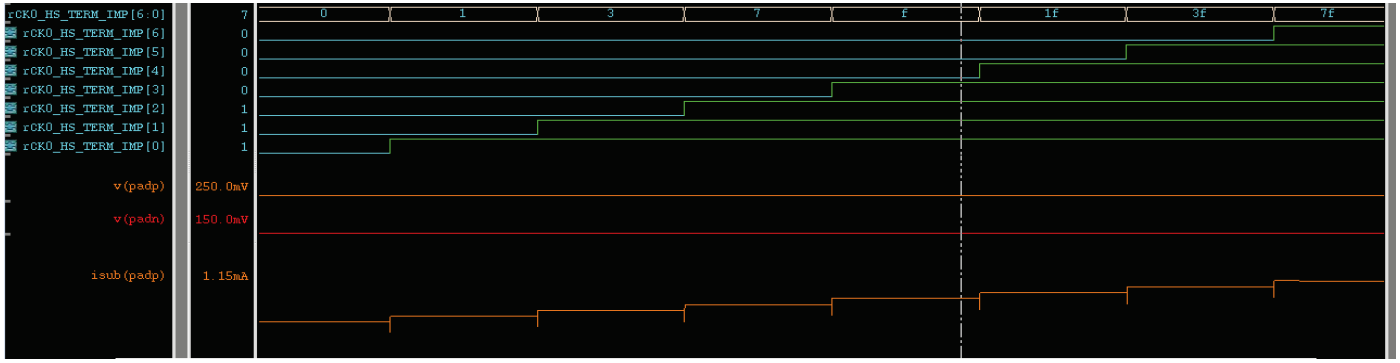
d) In each case, measure PAD voltage and PAD current and determine the termination resistance

```
always@(<tb_signal_for_CSR_Term_cfg_done>) begin
   if(Core_dft_pwr_intf.iPWRGD_PWROK===1'b1)  begin
      #<delay_value>;
      voltage_padp   = $snps_get_volt(<hierarchy>.PADP);
      voltage_padn   = $snps_get_volt(<hierarchy>.PADN);
      current_padp   = $snps_get_port_current(<hierarchy>.PADP);
      term_impedance = (voltage_padp - voltage_padn) / current_padp;
   end
 end
```

Application and Results (3/4)

Sample log file and waveform dump

```
UVM_INFO at  6015971: HS_TERM_IMP = 0, PADp(V) = 0.250000, PADn(V) = 0.150000,
PADp current = 0.000884 :: Term-impedance = 113.066436
UVM_INFO at  6916491: HS_TERM_IMP = 1, PADp(V) = 0.250000, PADn(V) = 0.150000,
PADp current = 0.000981 :: Term-impedance = 101.906082
UVM_INFO at  7817011: HS_TERM_IMP = 11, PADp(V) = 0.250000, PADn(V) =
0.150000, PADp current = 0.001067 :: Term-impedance = 93.686777
UVM_INFO at  8717531: HS_TERM_IMP = 111, PADp(V) = 0.250000, PADn(V) =
0.150000, PADp current = 0.001151 :: Term-impedance = 86.908291
...
```



Waveform plot showing the PAD voltage, CSR term_imp configuration, and PADp current draw

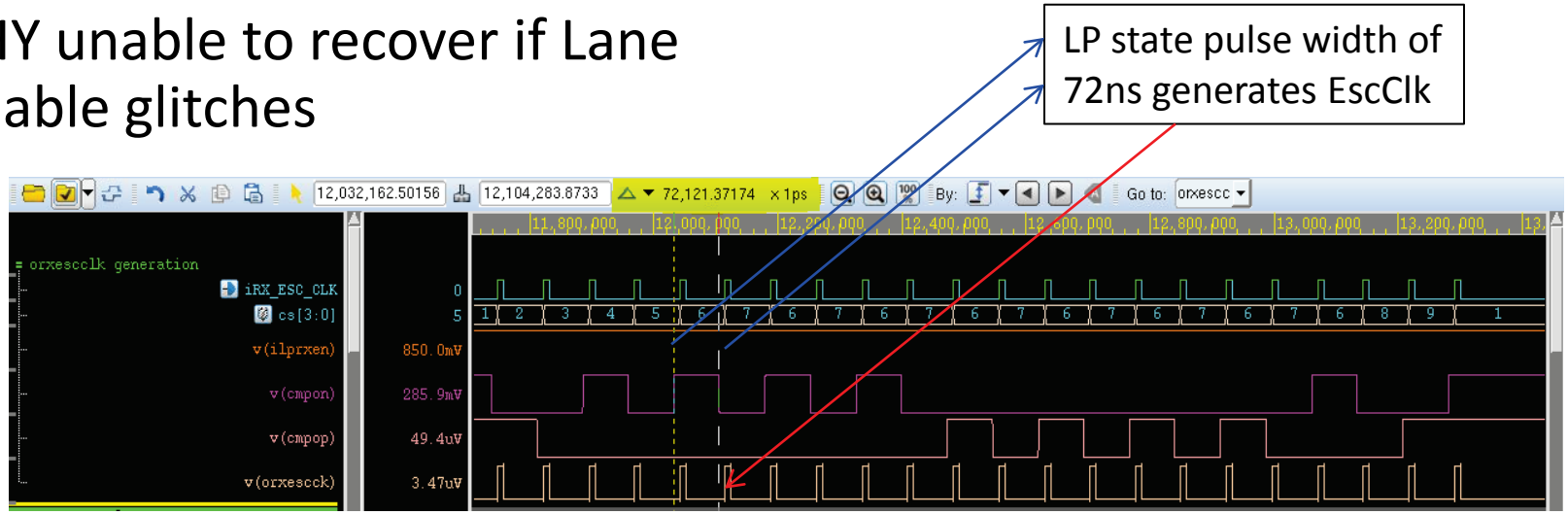
Results from Simulations (4/4)

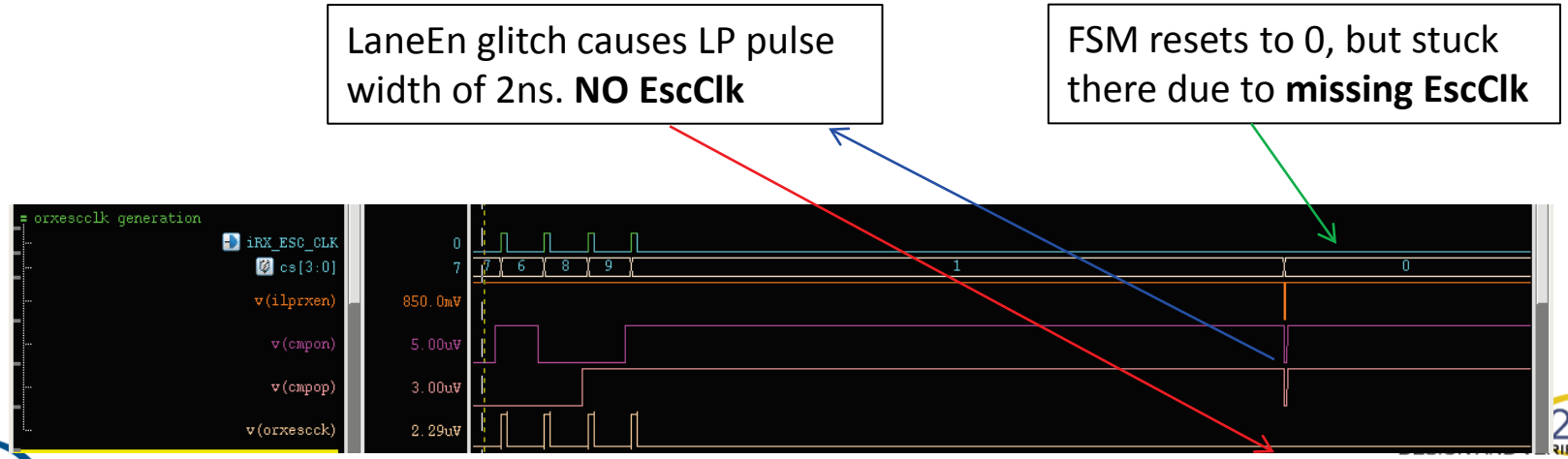
d) Validated proper design response to corner case scenarios

- For data bursts of different lengths and random payload data. The design was also validated to respond to error induced into bit sequences.
- Range of valid “data rates” supported by the DPHY standard for HS-Mode data transmission.
- Pulse width requirement: LP-Mode bit pattern validated was by varying the pulse width in the digital UVM testbench.
- Signal timing within the analog blocks (“clk-settle” time, as well as the “clk-miss” time parameters)

Key Issues Found

PHY unable to recover if Lane Enable glitches





Key Issues Found

Correlating RTL simulation and co-simulation results identified inaccuracies in RTL model of analog blocks in the modelling “clk-settle” and “clk-miss” parameters.

Conclusion

Advantages of the Co-simulation Setup

a) The UVM tb was effectively reused in cosim environment. Camera side stimulus, ScoreBoard checking and other protocol checks were reused as is.

b) Validated LP-Rx and HS-Rx functionality by simulating the transition between LP Mode → HS Mode → LP Mode.

c) Co-simulations are faster than full spice simulations. A full co-simulation run completes in 4 hours.

   - This enabled re-running a large number of tests that covered various random scenarios in the UVM tb, in the co-sim world.

Advantages of the Co-simulation Setup

e) Automatic checking/monitoring of ‘clk-miss’ and ‘clk-stl’ DPHY parameters with the help of the “checker probes”.

f) Automatic checking of termination resistance calibration in the digital UVM testbench and indicating pass / fail criterion.

Questions