INTRODUCTION (or REQUIREMENTS)

As a result of the consistent advances in the microelectronics technology, the integration of multiple computational units on a single chip had been possible. This brought about the concept of the System-on-Chip (SoC). SoC are often designed as customizable platforms, where the end-user can modify the architecture template to fit the needs of the target application. The increase in processor frequency and the exploitation of instruction level parallelism reaching their limits, multiprocessor architectures, named MPSoC were widespread. Design of MPSoC relies on methodologies and tools to help deal with both hardware and software aspects of the design. To cope with the challenge of designing MPSoCs under an increasing time-to-market pressure and the huge market competitiveness, Design Space Exploration (DSE) is highly essential in order to achieve shorter time-to-market with reasonably low cost of design. It consists of exploring a large number of different design decisions to find a set of optimal system designs that matches the user specifications and design constraints (Memory utilization, Energy Consumption, Performance on Hardware and Software, Communication Overhead, cost/area, and throughput). The term design space exploration (DSE) deals with system-level design problems such as hardware/software partitioning, application-architecture mapping. It is in general a multi-objectives optimization problem [6] that tries to find out one or several “optimal” design solutions based on multiple objectives regarding functional and non-functional properties such as correctness, execution time and power/energy consumption.

OBJECTIVES

We propose in this poster an hybrid approach for synthesis-estimation of MPSoC systems. This approach allows synchronizing the advancement of the synthesis stage and the performance estimation step. It is a model that establishes the interaction during the design phase of the models for estimating performance of analytical methods (such as graphs SDF) and methods of synthesis flows (such as simulation). We propose to exploit the performance metrics obtained by SDF graphs and integrate it into a hybrid model that ensures / guide the progress of the simulation in a stream of classical synthesis to limit the class of solutions architectures.

CONCLUSIONS

We have validated the proposed Codesign approach using a Motion JPEG decoder. We want to find an implementation of the MOTION JPEG decoder realizing 25 frames per second (fps) as a functional constraint and using 50MHz processors as a non-functional constraint. We are only interested in studying temporal performance depending on the three flowing aspects (1) thread execution time, (2) bus transfer rate and (3) the transfer primitive latency. The MOTION JPEG decoder reads a stream of JPEG images from an input peripheral: a traffic generator named TG and writes pixels on an output peripheral: a digital-to-analogue converter named RAMDAC. The first functional bloc DEMUX dispatches the input stream to the other blocs. The decoding chain begins with the decompression bloc (VLD), then the zigzag rearrangement bloc (ZZ), followed by the inverse quantification bloc (IQ). Finally, the stream passes to the inverse discrete cosine transformation (IDCT).

REFERENCES

[3] Imed BENNOU1 and Abderrazak JEMAI, Timed-SDF Constructions for Applications Throughput Analysis - 2011