

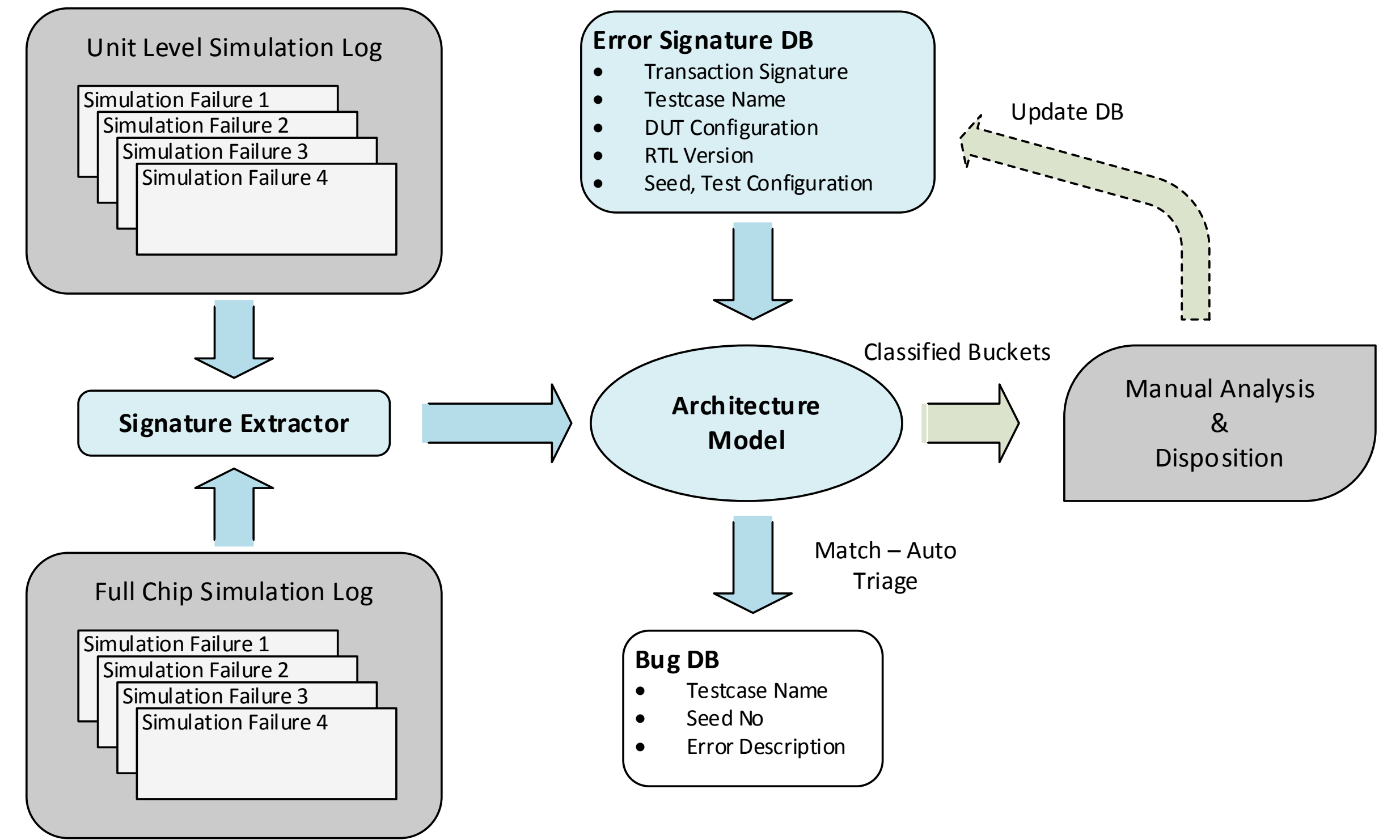
## PROBLEM STATEMENT

Pre-Silicon Debug at Chip Level takes considerable effort and consumes about 30% of chip design cycle time. Often bugs are sighted late in the design-cycle resulting in re-work, re-spin and tremendous cost to company.

Following are the objects of the Automation,

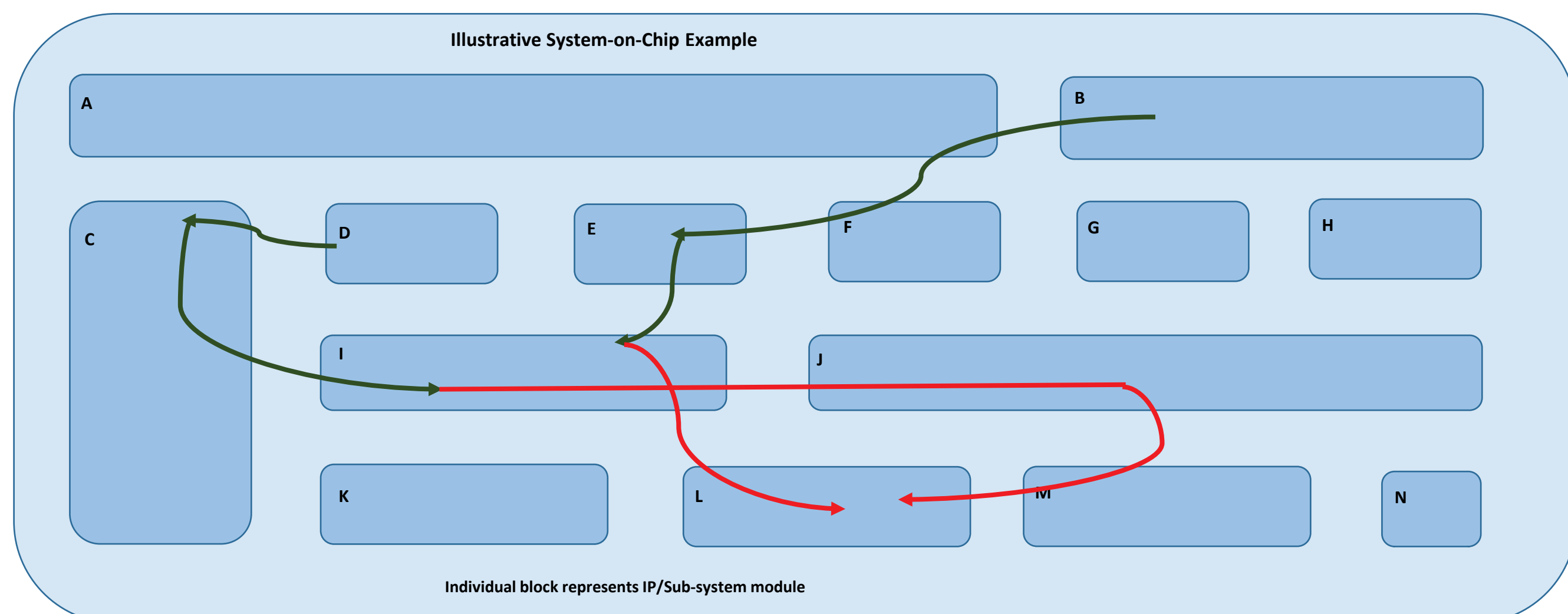
Objective	Method
Repository for failure Knowledge	If the failures are well documented in the tool, helps in easy coordination and communication.
Automatic Triaging	Reduce manual effort on well known signatures.
Meaningful Bucketing	Improve bucketing by incorporating architecture & transaction knowledge.
Assist in prioritization	Prioritize failures based on transaction types, signature frequency, DUT configuration etc.
Team Co-ordination	Need for efficient co-ordination and effective in cross-site communication.

## AUTOMATION ARCHITECTURE

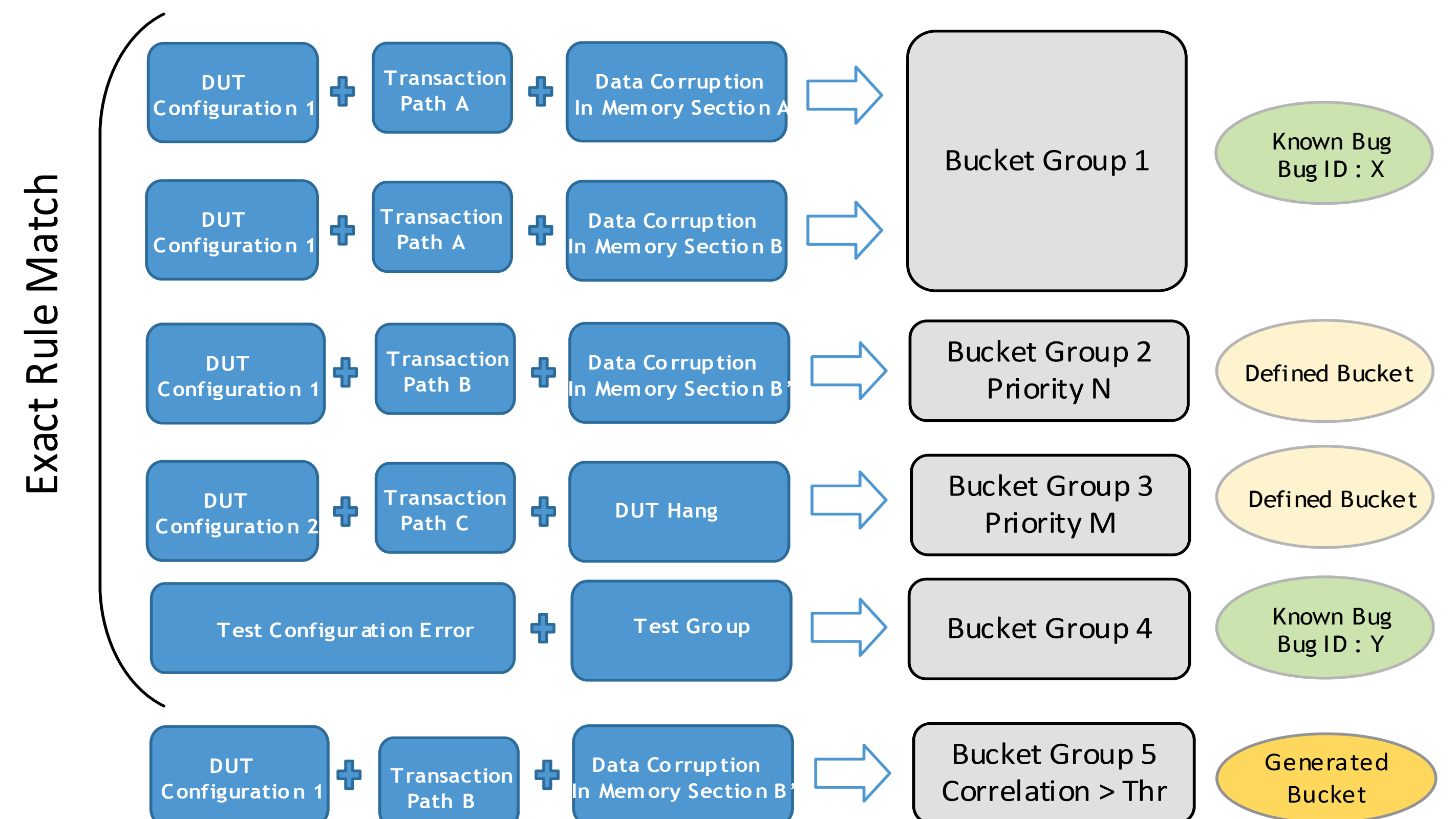


## Transaction Tagging – Key Enabler for Automation

- A Key enabler for automation is the ability to tag transaction in design and validation environment.
- Such tagged transactions reveal a trace which can be interpreted by the architecture model.
- The diagram shows two such fault traces in the SoC indicating potential fault in module I which can be used to classify the failure and auto-triage.

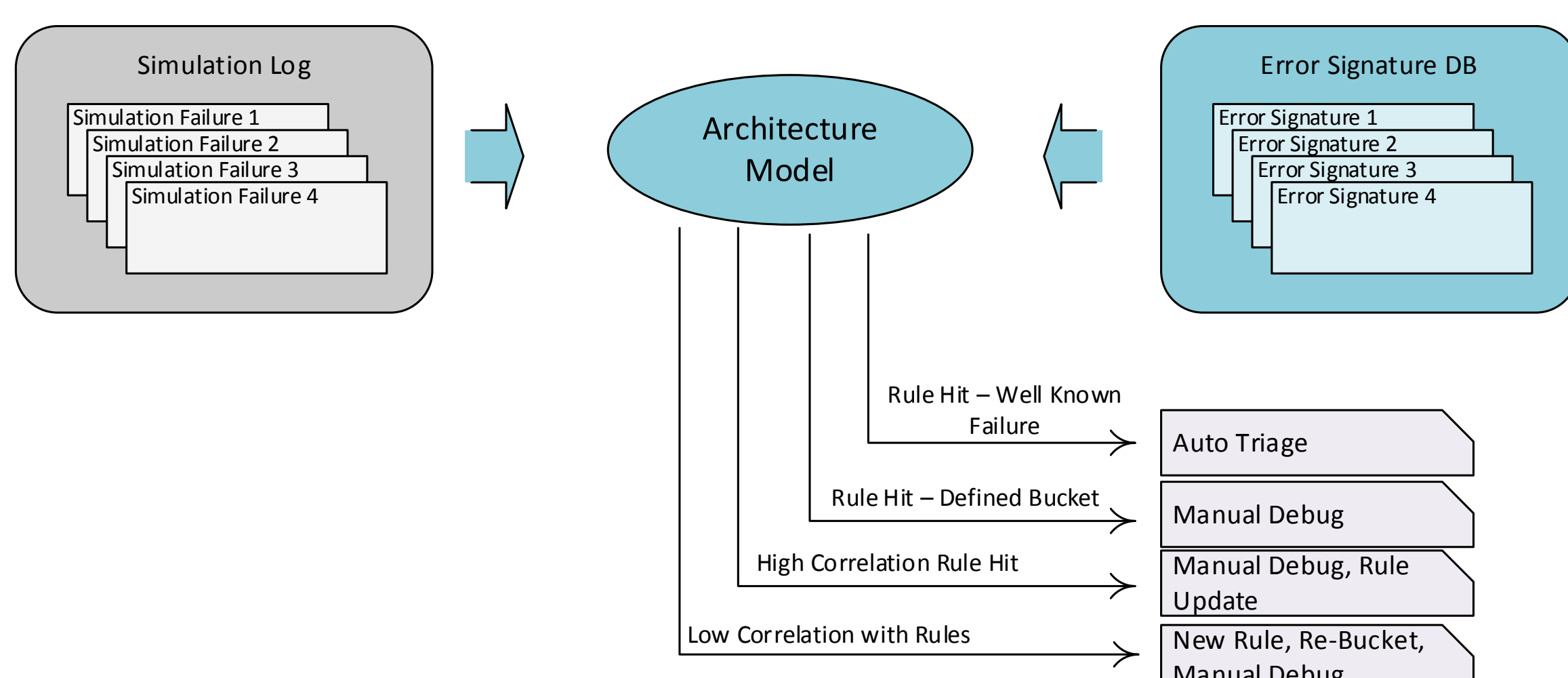


## Rule Based Architecture Model



## Search, Match, Update

- Known failures meta data (aka signature) is stored with in database.
- Rules are coded to indicate match with known signatures.
- Exact match triggers auto-triage.
- When Exact match is not present, match with high correlation is looked for.
- A high correlation leads to a new bucket entry formed.
- A low correlation index triggers manual entry creation in signature database.



## Over-all savings from method

Regression/Log Reports	Checker Error Based Classification	Signature Based Classification
<b>Number of Buckets in Typical Weekly Regression</b>	300 to 500	30 to 70
<b>Number of known buckets auto triaged</b>	10 to 15 (approx. 3%)	10 to 20 (approx. 30%)
<b>Number of buckets debugged every week</b>	150 to 200 (50% to 70%)	Usually 100%
<b>Life of bug in Full chip</b>	Typically between 3 to 5 weeks to record a new signature	Typically 1 week to record new signatures.
<b>Cross GEO co-ordination</b>	Every day stand-up meeting in morning , followed by late night sync-up in 1:1 with counterparts on debug progress	Thrice a week call, less frequent 1:1 sync-up on debug progress

## Reference

Efficient Failure Triage with Automated Debug: a Case Study Author: Sean Safarpour, Evean Qin, and Mustafa Abbas  
 Advanced Techniques for RTL Debugging Author: Yu-Chin Hsu , Bassam Tabbara , Yirng-An Chen , Fushing Tsai  
 From RTL to Silicon: The Case for Automated Debug Author: Andreas Veneris, Brian Keng, Sean Safarpour  
 Debug Limited No More: The Case for Debug Automation Author: Andreas Veneris