2015 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION INDIA

Sept 10-11, 2015
Bangalore, India

Conference Sponsor

accellera SYSTEMS INITIATIVE™

DVCON INDIA
CALL FOR PAPERS EXTENDED

The **Design and Verification Conference & Exhibition India** (DVCon India) is a highly technical conference in India targeting the application of standardized languages, tools, and methodologies for the design and verification of electronic systems, embedded systems and integrated circuits. Hosted by Accellera Systems Initiative, the format of DVCon India is similar to the successful DVCon United States conference held for over 10 years in the Silicon Valley.

The ultimate goal of DVCon India is to boost the interest, usage and development of electronic system designs. We look forward to users sharing the various challenges and solutions adopted by various teams across the industry. DVCon India also provides a much-needed platform to promote upcoming Electronic Design Automation (EDA) and Intellectual Property (IP) standards in India. This highly technical 2-day conference is organized to invite industry experts to learn and share best practices on:

- Modeling, Design and Verification of complex electronic systems at different levels of abstraction such as Virtual prototyping, Architectural Modeling, RTL, Emulation, HW acceleration, etc.
- The application of system-level design and verification languages such as SystemC and SystemVerilog
- Virtual Platform for Embedded Software Development
- Novel application of standard Design & Verification languages such as SystemVerilog, PSL, *e*, VHDL, etc.
- SoC Design Verification using the latest trends and methodologies such as UVM-SystemC, graph-based techniques, portable stimulus across block-subsystem-system all the way up to Post-Silicon
- Architectural Exploration at the early stage and High-level Synthesis
- The use of SystemVerilog Assertions (SVA), PSL and Formal Verification (Model Checking)
- Adoption of Universal Verification Methodology (UVM)
- Leveraging on legacy methodologies based on OVM, VMM and migration to UVM
- IP reuse, design automation and integration standards based on IP-XACT and SystemRDL
- Low-power design and verification using the Unified Power Format (UPF)

General topic areas on Electronic System Level (ESL), Virtual Platform, Verification & Validation, Analog/Mixed-Signal, IP reuse, Design Automation, and Low-power design and verification will be highlighted in tutorials, papers, and poster sessions.

Conference attendees are primarily designers of embedded systems, electronic systems, ASICs and FPGAs, as well as those involved in the research, development and application of EDA tools and IP integration solutions. The DVCon India conference attracts a highly skilled user base active in various industries focusing on research and development of automotive, aerospace, consumer, and wired and wireless communication products.

CALL FOR ABSTRACTS – ESL TRACK

DVCon India solicits presentations that are highly technical and reflect real life experiences in using languages, standards, methods and Electronic Design Automation (EDA) tools.

The ESL track aims to accelerate the adoption of SystemC in the Semiconductor Industry. It provides a platform for the SystemC beginners, SystemC/TLM experts, ESL managers and ESL vendors to share their knowledge, experiences & best practices about SystemC usage. Submissions are encouraged in (but not restricted to) the following topics:

- Transaction-level modeling for system-level design (VP, Multi-core, Performance, etc.)
- SystemC Language Development
- Verification Techniques using SystemC-UVM and VPI/PLI, DPI Interface
- Mixed-language environments involving SystemC and SystemVerilog/UVM
- SystemC Analog/Mixed-Signal Extensions & Power Modeling
- High-level synthesis from ESL languages SystemC/C++
- System-level design techniques, flows and methodologies
- Hardware/software/embedded co-design for early development
- HW/SW Co-Simulation and SoC Architecture Exploration
- Debugging Techniques and Configuration and Control in Platform Design

CALL FOR ABSTRACTS – DV TRACK

DVCon India solicits presentations that are highly technical and reflect real life experiences in using languages, standards, methods and Electronic Design Automation (EDA) tools.

In the DV Track we are soliciting detailed abstracts from industry leaders to share their ideas, thoughts and experiences in solving some of the most complex challenges in their respective fields of work/research. This track provides a platform for the wide Design-Verification community including beginners, architects/experts, managers and EDA vendors to share their knowledge, experiences and best practices about Design-Verification. Submissions are encouraged in (but not restricted to) the following topics:

- Using multiple HDLs and/or HVLs in a design cycle
- Novel application of existing standard DV (Design-Verification) languages such as SystemVerilog, PSL, *e*, VHDL, etc.
- Latest language developments in SystemVerilog
- Advanced stimulus generation methods, reuse of stimulus across levels of verification (portable stimulus)
- System-on-Chip Verification approaches to handle complexity, performance and reusability requirements
- Adoption of UVM
- Advanced techniques/features and extensions to UVM
- Real life applications of assertions using SVA and/or PSL
- Formal and semi-formal techniques, Assertion automation/synthesis
- Verification process and resource management
- Compliance and requirements-driven verification such as DO-254 standards
- Debug automation through transaction-level debug, smart tricks to handle performance issues, faster time to debug techniques
- Low Power intent verification through standards such as UPF and related technologies
- Usage of IPXACT and SystemRDL in design flow
- AMS challenges in Verification, usage of custom extensions to UVM/SystemVerilog to handle AMS related complexities

SUBMISSION GUIDELINES

Submit abstracts at: www.easychair.org/conferences/?conf=dvconindia2015

To spare you the many hours of preparation associated with other paper submissions, DVCon India has the following process:

- Submit a 500-1000 word abstract highlighting what you wish to present at DVCon India. The program committee will evaluate your abstract. The deadline for abstract submission is **Tuesday, July 15**.
- Authors of exceptionally strong abstracts will be shortlisted for oral or poster presentation at the conference. They will present their work at DVCon India on Thursday, September 10 or Friday, September 11.
- Consistent with the requirements for other DVCon presentations, ***your presentation may contain your company logo only on the title slide***.

An abstract is expected to include the following details:

1. A title
2. Name, affiliation, phone number and email addresses for all authors.
3. An introduction that specifies the context and motivation of the submission.
4. A summary of the specific contributions of your work.
5. A summary that highlights results. To evaluate your contribution, you must specify some results.
6. References, if appropriate

Your abstract can be at most two pages. You can format it in single or double column. Provide enough details so that the Technical Program Committee can evaluate the potential quality and interest of your possible presentation at DVCon India. **A one-paragraph summary will not fulfill this requirement.**

A template for the abstract is available on the DVCon India website.

2014 conference proceedings are available for download.

Please contact the Technical Program Committee if you have any questions on the submission process.

Important Dates:

Wednesday, July 15: Abstract submission deadline
Sept 10 (Thur) – Sept 11 (Fri): DVCon India conference

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DVCON INDIA
CALL FOR TUTORIALS EXTENDED

The **Design and Verification Conference & Exhibition India** (DVCon India) is a highly technical conference in India targeting the application of standardized languages, tools, and methodologies for the design and verification of electronic systems, embedded systems and integrated circuits. Hosted by Accellera Systems Initiative, the format of DVCon India is similar to the successful DVCon United States conference held for over 10 years in the Silicon Valley. This is DVCon India's second year.

The ultimate goal of DVCon India is to boost the interest, usage and development of electronic system designs. DVCon India is looking for tutorial topics that are current, have a high-level of interest and offer strong continuing educational content. Highly qualified engineers are expected to attend the sponsored tutorials during DVCon India 2015. Tutorial sponsorship allows companies to reach a captive audience during the half-day educational sessions and the opportunity to follow up with them during breaks, at the exhibits, and following the event. DVCon India is a highly targeted venue for engineers addressing major design and verification issues. You can position your company at the forefront of these discussions by sponsoring. **Submit proposals by July 15, 2015.**

Unlike other conferences, there is no extra charge for attending the tutorials. The presenter is virtually guaranteed a good attendance. Topics are:

- Modeling, Design and Verification of complex electronic systems at different levels of abstraction such as Virtual prototyping, Architectural Modeling, RTL, Emulation, HW acceleration, etc.
- The application of system-level design and verification languages such as SystemC and SystemVerilog
- Virtual Platform for Embedded Software Development
- SoC Design Verification using the latest trends and methodologies such as UVM-SystemC, graph-based techniques, portable stimulus across block-subsystem-system all the way up to Post-Silicon
- The use of SystemVerilog Assertions (SVA), PSL and Formal Verification (Model Checking)
- Adoption of Universal Verification Methodology (UVM)
- IP reuse, design automation and integration standards based on IP-XACT and SystemRDL
- Low-power design and verification using the Unified Power Format (UPF)

General topic areas on Electronic System Level (ESL), Virtual Platform, Verification & Validation, Analog/Mixed-Signal, IP reuse, Design Automation, and Low-power design and verification will be highlighted in tutorials, papers, and poster sessions.

Conference attendees are primarily designers of embedded systems, electronic systems, ASICs and FPGAs, as well as those involved in the research, development and application of EDA tools and IP integration solutions. The DVCon India conference attracts a highly skilled user base active in various industries focusing on research and development of automotive, aerospace, consumer, and wired and wireless communication products.

CALL FOR TUTORIALS – ESL TRACK

DVCon India – ESL track solicits detailed proposals for tutorials that are highly technical and reflect real life experiences in using languages, standards, methods and Electronic Design Automation (EDA) tools.

The ESL track aims to accelerate the adoption of SystemC in the Semiconductor Industry. It provides a platform for the SystemC beginners, SystemC/TLM experts, ESL managers and ESL vendors to share their knowledge, experiences and best practices about SystemC usage. Submissions are encouraged in (but not restricted to) the following topics:

- Virtual-Platforms and System-Level Design
  - Transaction-level modeling for system-level design
  - Hardware/software/embedded co-design
  - System-level design techniques, flows and methodologies
  - High-level synthesis from ESL languages
- Power
  - Low Power Design
  - Power estimation techniques
  - Power modeling
- Mixed-Signal (AMS)
  - SystemC AMS usage for mixed-signal simulation
  - AMS system-level and concept design

CALL FOR TUTORIALS – DV TRACK

DVCon India – DV Track solicits detailed proposals for tutorials from industry leaders in the field of Design & Verification. The DV Track provides a platform for the wide Design-Verification community including beginners, intermediate and seniors to learn the latest concepts, techniques, etc. in their respective domains of interest. Submissions are encouraged in (but not restricted to) the following topics:

- UVM – Universal Verification Methodology
- Latest language developments in SystemVerilog including:
  - New and enhanced constructs
  - Assertion enhancements
- Advanced stimulus generation methods, reuse of stimulus across levels of verification (Portable Stimulus)
- Formal Verification
  - Coding styles, techniques for assertions for formal
  - Model Checking techniques, target designs/blocks
- Compliance and Requirements-driven verification such as DO-254 and IS0 26262 standards
- Debug automation through transaction-level debug, smart tricks to handle performance issues, faster time to debug techniques
- Low Power intent verification through standards such as UPF and related technologies
- Use of IPXACT, SystemRDL in design flow
- Digital and Analog Mixed Signal (AMS) techniques
- Emulation, Acceleration, Prototyping

SUBMISSION GUIDELINES

Submit tutorial abstracts at: www.easychair.org/conferences/?conf=dvconindia2015

Tutorials are 90-minute sessions. DVCon India attendees have the opportunity to learn about different topics during the sessions. A tutorial may have a single speaker or several speakers. In either case, the submitter is responsible for organizing the tutorial.

If you are interested in providing a tutorial session, please submit your abstract via EasyChair by **July 15, 2015** and indicate that this is a tutorial submission. By submitting the tutorial proposal, you agree to become the tutorial sponsor.

A tutorial abstract is expected to include the following details:

- Abstract title stating that this is a tutorial submission
- Name, affiliation, phone number and email addresses for all speakers
- An introduction that specifies the context and motivation of the tutorial submission
- A summary of the specific content of your tutorial and your intended audience. For each presentation, mention the title and a short paragraph description.
- Must be descriptive enough to see what this tutorial will address and what the attendees would learn from it
- Maximum 3 pages

There is no template for the proposal; use the default Word template.

- Provide enough details so that the Technical Program Committee can evaluate the potential quality and interest of your possible tutorial at DVCon India.
- Please submit your proposal via EasyChair by **July 15, 2015**.

Tutorial roles

Tutorial Organizer: For the selected tutorial, the Organizer coordinates all tutorial activities with DVCon India, including ensuring that content is delivered in a timely manner and that the final presentation goes smoothly; follow-through is critical, the Organizer must interact with the Tutorial Chair.

- The Organizer writes the proposal for the tutorial and the abstract that is submitted for proposal evaluation.
- The Organizer selects and confirms the participation of the Presenter(s) (who could include the Organizer).
- The Organizer writes the material that will be included in the website and publications. It is very important that the Organizer write the material to help a potential attendee decide if they should attend this tutorial.
- The program material should describe the target audience and their expected level of familiarity with the topic (Expert/Intermediate/Beginner).
- An Organizer can propose multiple tutorials on aligned topics with different speakers.

Presenter: The Presenter is responsible for delivering the presentation.

Important Dates:

- **July 15:** Tutorial submission closes
- **July 31:** Tutorial accept/reject notification
- **August 15:** Deadline to submit final tutorial description, title, and presenter information for DVCon India website and publications
- **August 22:** Accepted presenters agree to register for the conference and submit a copyright form
- **August 22:** Deadline to submit presentation slides
- **September 10-11:** DVCon India 2015 conference

Questions?

Feel free to contact the Tutorial Chair, Pradeep Salla, at pradeep_salla@mentor.com for questions on the submission process.

DVCon India reserves the right to restructure all tutorial suggestions.