Conference Program at a Glance

Day 1: Thursday, September 10, 2015

Time	Royal Ball Room	Kamal	Grand Ball Room	Diya	Sitara
	Grand Ball Room D1M2-ESL				
9:30 - 9:45	Opening Talks/Lamp Lighting				
9:45 - 10:30	**Keynote Speech** Harry Foster, Chief Scientist, Design Verification Technology Division, Mentor Graphics Title: From Growing Complexity to Faster Horses				
10:30 - 11:00	**Invited Keynote** Vinay Shenoy, Managing Director, Infineon Technologies India Pvt. Ltd Title: "Make in India" Implies Innovate-Engineer-Manufacture				
11:00 - 11:30	Tea Break & Networking				
11:30 - 12:30	Royal Ball Room D1M2-ESL		Grand Ball Room D1M2-DV		
	Keynote Speech Vladimir Ivanov, LG Electronics Title: Reconfigurable Radio Design and Verification - A System Level Design Case Study		**Keynote Speech** Nick Heaton, Cadence		
	Invited Talk Pankaj Singh, Infineon Title: Ensuring Verification Quality for Next Generation Automotive SoC's: System's Approach		**Panel Discussion** Title: IoT Verification: Cubbon Park or Jurassic Park		
12:30 - 13:30	Lunch Break				
13:30 - 15:00	Royal Ball Room D1A1.1-ESL	Kamal D1A1.2-ESL	Grand Ball Room D1A1.1-DV	Diya D1A1.2-DV	Sitara D1A1.3-DV
	ESL Tutorials		**DV Tutorials**		
	Title: Early Architecture Exploration leveraging TLM2.0: Challenges & Opportunity Synopsys	Title: SystemC Updates (13:30 - 14:00) Accellera Title: TLM 2.0 Tutorial (14:00 - 15:00) Accellera	Title: Addressing SOC /IP Verification Framework Creation with UVM-Centric Mechanisms Synopsys	Title: Creating SystemVerilog UVM Testbenches for Simulation and Emulation Platform Portability to Boost Block-to-System Verification Productivity Mentor Graphics	Title: Advanced Debug for SoC Verification Cadence
15:00 - 15:30	Tea Break & Networking				
15:30 - 17:30	Royal Ball Room D1A2.1-ESL	Kamal D1A2.2-ESL	Grand Ball Room D1A2.1-DV	Diya D1A2.2-DV	Sitara D1A2.3-DV
	Invited Talk Dr. Sacha Loitz, Continental		**Panel Discussion** Supporting the Evolving Verification Flow		
	ESL Accellera Tutorials		**DV Tutorials**		
	Title: Leveraging Portable Stimulus across Domains and Disciplines Mentor Graphics, CVC, Breker & Vayavya Labs	Title: IP-XACT Tutorial (16:00 - 16:45) Prashant Karandikar Title: UVM-SystemC (16:45 - 17:30) Anupam Bakshi, Agnisys	Title: Expediting the Code Coverage Closure using Static Formal Techniques – A Proven Approach at Block and SoC Levels! Mentor Graphics	Title: Software driven Verification at the SoC Level Cadence	Title: FPGA Implementation Validation and Debug Mentor Graphics
	Grand Ball Room D1E1				
17:30 - 21:00	**Evening Activities – Gala Dinner** Drinks & Snacks Celebrating 10 Years of SystemVerilog UVM Standardization with IEEE External Performers Dinner				

Day 2: Friday, September 11, 2015

Time	Royal Ball Room	Kamal	Grand Ball Room	Diya	Sitara
8:00 - 8:45	Portable Stimulus Birds-of-a-Feather				
	Grand Ball Room D2M1				
9:30 - 9:35	Opening Talks				
9:35 - 9:45	Accellera Overview				
9:45 - 10:30	**Keynote Speech** Manoj Gandhi, Executive Vice President and General Manager, Verification Group, Synopsys Title: Propelling the Next Generation of Verification Innovation				
10:30 - 11:00	**Invited Keynote** Atul Bhatia, Founder & Former CEO, nSys Title: Opportunities for Semiconductor Design Startups in India				
11:00 - 11:30	Tea Break & Networking				
11:30 - 13:00	Royal Ball Room D2M2-ESL		Grand Ball Room D2M2.1-DV	Diya D2M2.2-DV	Sitara D2M2.3-DV
	ESL Panel Discussion		**DV Papers** UVM/SV	Emulation, FPGA & Acceleration	Portable Stimulus, GBV, Coverage
	Title: ESL Continuum – Architecture --> S/W Development --> Post-Silicon Validation and Calibration Moderator: Amit Garg, Synopsys Panelists: Bishnupriya Bhattacharya, Cadence Ruchir Dixit, Mentor Graphics Saurabh Tiwari, Intel Prasanna Kesavan, Broadcom Abhilash, NVIDIA Amit Sethi, Synopsys		Title: 24 – UVM RAL: Registers on demand – Elimination of the Unnecessary Speaker: Sailaja Akkem, Microsemi	Title: 53 – FPGA Prototyping the Next Generation Tegra SoC – 50x Speed over Emulation SpeakerS: Sivarama Prasad Valluri and Ramanan Sanjeevi Krishnan, NVIDIA	Title: 118 – Walking the Graph SpeakerS: Sandeep Korrapati, Holger Horbach, Klaus Keuerleber and Alexander Jung, IBM
			Title: 25 – Extending a Traditional VIP to Solve PHY Verification Challenges SpeakerS: Amit Tanwar and Manoj Manu, Mentor Graphics	Title: 138 – Framework for holistic assessment of Potential Performance Gains with different Simulation Acceleration modes SpeakerS: Parag Goel, Amit Sharma and Adiel Khan, Synopsys	Title: 76 – Network Packet Header Generation Using Graph-Based Techniques combined with Software Testing Strategies Speakers: Sridevi Navulur, Satheesh Parasumanna, Xilinx and Rama Chaganti, Mentor Graphics
			Title: 73 – Software Driven Hardware Verification – A SystemVerilog DPI/UVM-Based Approach Speakers: Milan V. Purohit, Santanu Bhattacharyya, Solarflare, Puneet Goel, Coverify and Amit Sharma, Synopsys	Title: 82 – Recipes for Better Simulation Acceleration Performance Speakers: Anoop Hc, Vijayakrishnan Rousseau and Gaurang Nagrecha, Intel	Title: 111 – Coverage Closure – Is it a "Game of Dice" or "Top 10 Tests" or "Automated closure"? Speakers: Nagasundaram Thillaivasagam, Nikhita Raj J, Nitin Kumar Muthuselvan and Aditya Sharma, VerifLabs
13:00 - 14:00	Lunch Break				
14:00 - 15:30	Royal Ball Room D2A1.1-ESL	Kamal D2A1.2-ESL	Grand Ball Room D2A1.1-DV	Diya D2A1.2-DV	Sitara D2A1.3-DV
	ESL Papers		**DV Papers** UVM/SV	ABV, Formal, CDC	SoC & Stimulus Generation
	Title: 35 – Leveraging ESL Approach to Formally Verify Algorithmic Implementations Speakers: Achutha Kirankumar V M, Bindumadhava S, Aarti Gupta and Disha Puri, Intel	Title: 134 – A Methodology for Interrupt Analysis in Virtual Platforms Speaker: Puneet Dhar, Synopsys	Title: 54 – The Art of Writing Predictors Efficiently using UVM Speakers: Dolly Mehta and Jeremy Ridgeway, Avago	Title: 87 – A Method to Accelerate SoC Implementation Cycle by Automatically Generating CDC Constraints Speakers: Sulabh Kumar Khare and Ashish Hari, Mentor Graphics	Title: 83 – Stimulus Generation for Functional Verification of Memory Systems in Advanced Microprocessors Speakers: Vaibhav Ashtikar, Bhanupratap Singh Chouhan, Nagesh Vishnumurthy, Krishnakumar Ranganathan, Broadcom & Basavaraj Talawar and Vani M. NITK, Surathkal
	Title: 148 – Achieving Real-Time Performance for Algorithms on Application-Specific SOC using TLM Modeling Speakers: Baljinder Singh Sood, Sharath Naidu, Saurin Patel and Pushkar Sareen, Freescale	Title: 41 – Pre-Silicon Host-based Unit Testing of Driver Software using SystemC Models Speakers: Somarka Chakravarti, Aravinda Thimmapuram, Tamal Saha and Rathina Thalaiappan, Intel	Title: 88 – Generic Verification Infrastructure around Serial Flash Controllers Speakers: Harsimran Singh, Snehlata Gutgutia and Chanpreet Singh, Freescale	Title: 97 – Challenges with Power Aware Simulation and Verification Methodologies Speakers: Divyeshkumar Vora, Venkatesh Bharathi, ARM & Srikanth Nuni, Jayarama Navada and Vinay Kumar Singh, Mentor Graphics	Title: 66 – Using a Generic Plug and Play Performance Monitor for SoC Verification Speakers: Kaushal Modi, Janak Patel, Bhavin Patel, Ajay Tiwari and Ambar Sarkar, eInfochips
	Title: 89 – Vlang, a System Level Verification Perspective Speaker: Puneet Goel, Coverify	Title: 30 – MeSSMArch – A Memory System Simulator for Hardware Multithreading Architectures Speaker: Sushil Menon, NVIDIA	Title: 6 – A UVM Based Methodology for Processor Verification Speakers: Abhineet Bhojak and Tejbal Prasad, Freescale	Title: 37 – Enabling Shift-Left through FV Methodologies on Intel Graphics Designs Speakers: Achutha Kirankumar V M, Aarti Gupta, Bindumadhava S and Aishwarya R, Intel	Title: 47 – Transactional Memory Subsystem Verification for an ARMv8 server class CPU Speakers: Ramdas Mozhikunnath, Parveez Ahamed, Brijesh Reddy and Jayanto Minocha, APM
15:30 - 16:00	Tea Break & Networking				
16:00 - 17:30	Royal Ball Room D2A2.1-ESL	Kamal D2A2.2-ESL	Grand Ball Room D2A2.1-DV	Diya D2A2.2-DV	Sitara D2A2.3-DV
	ESL Papers		**DV Papers** UVM/SV	AMS	SELECTED TOPICS
	Title: 113 – Making Virtual Prototypes Work – A Case Study Speakers: Jigar Patel, Kartik Jivani and Ambar Sarkar, eInfochips	Title: 130 – A Methodology for Using Traffic Generators with Real-Time Constraints Speaker: Avinash Mehta, Synopsys	Title: 131 – Has the Performance of a Sub-system been Beaten to Death? UVM Framework does it ALL!!! Speakers: Subhash Joshi, Sangaiyah Pandithurai and Manohar Vaddineni, Qualcomm	Title: 84 – Analog Mixed-Signal Verification at SOC Level: A Practical Approach for the use of Verilog-AMS vs. SPICE Views Speakers: Gautham Harinarayan, Nitin Pant and Manmohan Rana, Freescale	Title: 145 – Intelligent Coverage Driven, Modern Verification for VHDL Based Designs in Native VHDL with OSVVM Speakers: Juhi J, Vecima Networks, Anupam Maurya, Vijay Mukund Srivastav and Prabhat Kumar, CVC
	Title: 105 – Dynamic Configuration of SystemC Models Speakers: Shruti Baindur, Simranjit Singh and Anand Patil, Infineon	Title: 40 – Development of a Virtual Platform for Software Enablement and Hardware Verification Speakers: Sandeep Jain, Rajesh Jain, Sourav Roy and Sumail Singh Brar, Freescale	Title: 149 – Beyond UVM Registers – Better, Faster, Smarter Speakers: Rich Edelman and Bhushan Safi, Mentor Graphics	Title: 122 – Challenges in Mixed Signal Verification Speakers: Amlan Chakrabarti and Sachin-Sudhakar Kulkarni, AMD	Title: 86 – MIPI M-PHY Analog Modeling with Verilog-AMS (Wreal) and Verification using SV/UVM-MS Methodology Speakers: Mallikarjuna Reddy Y, Venkatramanarao K and Somanatha Shetty A, TVS
	Title: 58 – Verification Techniques for CPU Simulation Model Speakers: Gaurav Sharma, Navya Prabhakar, Circuitsutra & Sandeep Jain, Freescale	Title: 33 – Design & Verify Virtual Platform with Reusable TLM 2.0 Speaker: Ankush Kumar, 3DIPSemi	Title: 8 – How To Improve Our Verification Productivity – From Migration to Checking Consistency Speaker: Namphil Jo, Marvell, Korea	Title: 81 – PHY IP Verification – Are Conventional Digital DV Techniques Sufficient? Speaker: Somasunder Sreenath, Cadence	Title: 100 – Absolute GLS Verification – A method that Enables Early Simulation of STA Constraints Through Gate Level Simulation Speakers: Deepak Mahajan, Ateet Mishra and Shiva Belwal, Freescale
	Hallways		Hallways		
	ESL Posters		**DV Posters**		
	91 – VirtualATE: SystemC Support for Automatic Test Equipment. Nitin Garg, Shabarish Sundar, Continental, Amarnatha Reddy, CircuitSutra, Marapa Reddy, CircuitSutra and Sacha Loitz, Continental 132 – VP Quality Improvement Methodology. Meghana Moorthy, Melwyn Scudder and Kartik Shah, Intel 144 – Hybrid Emulation Practical Use Cases. Sylvain Bayon de Noyer, Synopsys		94 – Thinking Beyond the Box: Adopt the Reusable UVM Thread Management and Customized UVM Reset Package to Attack Thread Aware Verification Challenges. Roman Wang, AMD and Uwe Simm, Cadence 72 – A Reusability Combat in UVM: Callbacks vs Factory. Vikas Billa, Deepak Kumar E V, Sathish Dadi and Ranganath Kempanahally, elitePLUS 27 – Static Power Intent Verification of Power State Switching Expressions. Srobona Mitra, Bhaskar Pal, Soumen Ghosh, Rajarshi Mukherjee and Kaushik De, Synopsys 115 – A Unified Framework for Multilanguage Verification IPs Integration. Selva Kumar Krishnamoorthi, Surinder Sood, and Gaurav Jalan, Smartplay 3 – Verification of ARC Processor Core using Certitude for ISO 26262 Verification. Vikas Bhandari, Synopsys 79 – Addressing the Challenges of ABV in Complex SOCs. Rithin A N, Arif Mohammed and Rupinjeet Marwah, TI 38 – Increase Productivity with Reflection API in Design Verification. Shivayogi Kerudi, Vijay Mukund Srivastav, Vani S, CVC and Dr. Brad Quinton, Invionics 45 – Methodology for Hardware Software Co-verification of Video Systems on Pre- and Post-Silicon. Vinesh Peringat, Xilinx 60 – Driving Analog Stimuli from a UVM Testbench. Amlan Chakrabarti and Satvika Challa, AMD 136 – Dynamic Power Automation UVM Framework. Raghavendra Jn, Harathi Gudidevuni and Nikhil Gupta, Qualcomm 147 – Complementing Verification of Highly Configurable Design with Formal Techniques. Manik Tyagi and Deepak Jindal, Qualcomm		
	Grand Ball Room D2A3				
17:30 - 18:00	Closing Ceremony & Awards				