Advanced Debug for SOC Verification Tutorial

[Indago™ Debug Platform Overview]

cadence®
Debugging Continues to be the Most Time Consuming Effort by 50%

And it’s getting worse. WHY ???

- Same Debug Methodology for 20 years
  *While there has been very good progress in improving all other areas of verification, very little has been done in Debug automation*

- Increasingly larger SoC designs and many debug iterations producing Terabytes of Data
  *Finding the source of the bug is becoming like finding “a needle in a hay stack”*
What would you do if you were given 25% of your TIME back?

*Cadence set out to do exactly that*

**But HOW ???**

- **Debug platform architected from the ground up**
  - Leveraging the latest in s/w database architecture as its foundation of a common framework for performance, extensibility, and scalability

- **Platform extensibility, scalability, and integration**
  - User-selected Apps covering various functional verification tasks to view and debug from IP-to-SoC level across functional teams

**Today's Verification Effort**

- 25% TIME Savings
- 25% Debug
- 10% Coverage analysis
- 5% Test planning
- 10% Test creation
- 5% Test execution

**Patented Root Cause Analysis (RCA) Technology and BIG Data Techniques**

- Leverage patented RCA technology together with BIG Data techniques to quickly find the source of the bug
Introducing Cadence® Indago™ Debug Platform

Finding the **Source of the Bug** after **One Debug Run** is NO Longer a Dream

**Traditional Debug Flow**

1. Code
2. Sim
3. DB
4. Debug

**Indago™ Debug Flow**

1. Code
2. Sim
3. DB (Waveforms, log messages, code execution – “Big Data”)
4. Debug

**Time savings***

*As seen by customers

**DEBUG PRODUCTIVITY** 2x - 3x

“Cadence’s Indago Debug Analyzer App has improved our debug productivity up to 50 percent because it helps us find the root cause of the bugs faster with features like reverse debugging. We believe the Indago Debug Platform will enable us to continue to deliver for applications including consumer electronics, fitness tracking, wearables and IoT.”

Robert Richter, Senior Expert, ASIC Development, at Bosch
Key Benefits of Cadence® Indago™ Debug Platform

A Paradigm Shift in Debug Methodology Cutting Debug Time in ½

- **2X debug productivity improvement with Indago through:**
  - Patented Root Cause Analysis technology
  - BIG Data concepts for intelligent automation
  - Integrated Analysis GUI scalable from IP-to-SoC level debug

- **3 Indago platform Apps addressing specific debug tasks**
  - Debug Analyzer: RTL/GL and Testbench
  - Embedded Software Debug: Synchronized ESW/HW
  - Protocol Debug: Interface protocol functional validation

- **Supports Cadence and 3rd party verification engines**
  - Debug Analyzer: Phased RTL/TB support through next several releases
  - Embedded SW: Today (unmodified TARMAC trace files)
  - Protocol Debug: Today (for supported protocols)
Competitors Debug Solutions

RCA on RTL Only

• Competitors provide RCA on RTL/GL design only
  – RTL only one piece of the debug picture

• Engineers are forced to debug with severely limited visibility into other aspects of the environment
Indago™ Root Cause Analysis

RCA across all aspects of the simulation

Causal Relationships to explore

Jump to RC of value changes

RCA Engines

Messaging DB
Embedded SW DB
TB/RTL Source Execution DB
VIP DB
Embedded SW RTL/GL Testbench SystemC Waveform DB Debug DB
Indago™ Root Cause Analysis

RCA across all aspects = increased recording

Causal Relationships to explore

Jump to RC of value changes

RCA Engines

Messaging DB
Embedded SW DB
TB/RTL Source Execution DB
VIP DB
Waveform DB
Debug DB

Indago Root Cause Analysis

Root Cause Analysis (RCA)

Indago™ provides a comprehensive Root Cause Analysis (RCA) solution that supports RCA across all aspects of your design. This increased recording capacity enables deeper exploration of causal relationships and quicker identification of root causes of issues.

Key features include:
- RCA Engines for various domains:
  - Messaging DB
  - Embedded SW DB
  - TB/RTL Source Execution DB
  - VIP DB
  - Waveform DB
  - Debug DB
- Embedded SW Testbench
- RTL/GL SystemC

Indago™ supports a wide range of system development stages, from early design inception to final verification, ensuring a holistic approach to problem-solving.

Accellera Systems Initiative

Design and Verification Conference and Exhibition (DVCon) India 2015
Indago™ Root Cause Analysis

RCA across all aspects = increased recording

Indago Big Data

*(when compared to traditional debug)*
Indago™ Big Data Analysis

What makes Indago unique

• Recording additional data allows for powerful analysis capabilities such as:
  – Root Cause Analysis (RCA)
    • RCA Component
    • Direct Access
  – Playback Debugger
  – SmartLog
  – SmartPrint
  – Time Tables
  – Powerful Searching
  – Call stack analysis
  – Variables Table

• Let’s take a closer look at some of these features now …
Indago™ Debug Platform

Unified Analysis GUI

- Debug data from all sources visualized in the same GUI
  - Eliminates GUI context switching
  - Consistent debug experience
  - Quick ramp up

- Unified RCA across debug data sources
- Complete synchronization
- App specific customization

Messaging DB  Embedded DB  SW  TB/RTL  VIP  Waveform DB  Debug DB
Source Execution DB
Indago™ Apps

• Apps are individual products targeted at a specific debug task
  – Indago Debug Analyzer App: RTL/GL/TB debug
  – Indago Embedded SW Debug App: Embedded SW/HW Debug
Indago™ Debug Analyzer App DEMO
Demo Scenario

- Ran a regression of 100 test on the “CLAB” project
- Overall 25 tests failed
- 14 tests failed on parity mismatch error
- Picked the shortest parity mismatch test to debug
Demo environment Basics (CLAB)

- Mixed VHDL and Verilog design
- System Verilog VE
- Three input interfaces
  - Serial packets IF (drives packets byte by byte)
  - Parallel packets IF (drives packets in one cycle)
  - Register IF (used for configuring the DUT)
- One output interface
  - Multi packets IF (drives packets in one cycle with parity)
Failing Scenario

- Expected Parity calculation
- Parity Mismatch

Parallel packet
Multi packet

Add
Predict
Match

Parallel IF
Serial IF

Parallel packet driven

UVM Scoreboard

Parity calculation

Registers
DUT

Add 32

Parallel packet
Multi packet

In FIFO
In Mux
Muter
Limiter
Parity
Inverter
Out FIFO
Out Mux
Out FIFO
Arbiter

Add 32

Parallel packet driven

In FIFO
In Mux
Muter
Limiter
Parity
Inverter
Out FIFO
Out Mux
Out FIFO
Arbiter

Add 32
Demo debug Objectives

- VE developer debugging
- In this session
  - Understand the what random configuration was generated
  - Explore the VE parity calculation
  - Explore the DUT parity calculation
  - Compare the 2 parity algorithms
  - Assign session to designer upon DUT bug
Indago™ Embedded Software Debug App DEMO
Unified Embedded Software Debug Across Platforms and Processor Model Abstractions

- Unified embedded software debug for all Cadence platforms
- Unified embedded software debug for all processor abstractions
  - Fast processor models, RTL (simulation), RTL (emulation)
- Post-process (now) and interactive software debug (future)
- Multi-core and multi-processor
- Hardware/software co-debug
- Bare metal to OS software debug

Unified Embedded Software Debug Engine

TLM/RTL Hybrids
(Virtual Prototype with RTL)

Incisive® Functional Verification Platform
(Simulation)

Palladium® Verification Computing Platform
(Emulation)
Indago ESWD App Flow

1. Compile and Run
2. Generate Database
   Respond to Queries
3. Debug Offline
DEMO Design: HAMSA SoC – CPU Subsystem
Embedded SW Debug Scenario

• **Environment:**
  – 4 ARM A53 Cores
  – Several Peripherals, including 4 UART Interfaces

• **Failing Scenario:**
  – Each core should write an output message through its corresponding UART interface to signify that booting is complete
  – We are receiving character ‘C’ twice on UART3 (scoreboard test in testbench would catch this)
  – We are not receiving any message from CPU2 on the UART2 interface

• **To Debug:**
  – Examine HDL signals
  – Examine Embedded SW code execution
  – Single step
  – Examine functions and variables values
Indago™ Protocol Debug App

Next-generation protocol debug aid

- Simplifies debug by illuminating design and VIP behavior
- Support for many popular protocols in 2015, others to follow
- Seamless integration with all major simulators
Summary: New Cadence® Indago™ Debug Platform

✓ **2X** debug productivity improvement
  • Indago Debug Platform CUTS Your DEBUG TIME in HALF
  • Gain more TIME back in your LIFE
  • Customers* are seeing these benefits today!

✓ **3 Apps** addressing specific debug tasks
  • RTL/GL and Testbench
  • Synchronized ESW/HW
  • Interface protocol functional validation
  • *More Apps to come*

✓ **Available Today!**

*Customers like Renesas, Siemens, and TI presented about their success at CDNLive. ST has a success story published on Cadence.com.