2017 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION INDIA

DVCon India 2017

September 14-15, 2017
The Leela Palace, Bangalore, India

CALL FOR TUTORIALS

The Design and Verification Conference & Exhibition India (DVCon India) is a highly technical conference in India targeting the application of standardized languages, tools and methodologies for the design and verification of electronic systems, embedded systems and integrated circuits. Hosted by Accellera Systems Initiative, the format of DVCon India is similar to the successful DVCon United States conference held for over 10 years in the Silicon Valley.

The ultimate goal of DVCon India is to boost the interest, usage and development of electronic system designs. DVCon India is looking for tutorial topics that are current, have a high-level of interest and offer strong continuing educational content. Highly qualified engineers are expected to attend the sponsored tutorials during DVCon India 2017. Tutorial sponsorship allows companies to reach a captive audience during the half-day educational sessions and the opportunity to follow up with them during breaks, at the exhibits, and following the event. DVCon India is a highly targeted venue for engineers addressing major design and verification issues. You can position your company at the forefront of these discussions by sponsoring a tutorial. **Submit proposals by May 19, 2017.**

Unlike other conferences, there is no extra charge for attending the tutorials. The presenter is virtually guaranteed a good attendance.
A few topics are:

- Modeling, Design and Verification of complex electronic systems at different levels of abstraction such as Virtual prototyping, Architectural Modeling, RTL, Emulation, HW acceleration, etc.
- The application of system-level design and verification languages such as SystemC, SystemVerilog
- Virtual Platform for Embedded Software Development
- SoC Design Verification using the latest trends and methodologies such as UVM-SystemC, graph-based techniques, portable stimulus across block-subsystem-system all the way up to Post-Silicon
- The use of SystemVerilog Assertions (SVA), PSL and Formal Verification (Model Checking)
- Adoption of Universal Verification Methodology (UVM)
- IP reuse, design automation and integration standards based on IP-XACT, SystemRDL
- Low-power design and verification using the Unified Power Format (UPF)

General topic areas on Electronic System Level (ESL), Virtual Platform, Verification & Validation, Analog/Mixed-Signal, IP reuse, Design Automation, and Low-power design and verification will be highlighted in tutorials, papers and poster sessions. Conference attendees are primarily designers of embedded systems, electronic systems, ASICs and FPGAs, as well as those involved in the research, development and application of EDA tools and IP integration solutions. The DVCon India conference attracts a highly skilled user base active in various industries focusing on research and development of automotive, aerospace, consumer, and wired and wireless communication products.

General Chair
Prasanna Kesavan
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Tutorial Chair
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accellera SYSTEMS INITIATIVE™

Sponsor: Accellera Systems Initiative is an industry consortium with a mission to provide design and verification standards required by systems, semiconductor, IP, and design tool companies to enhance a front-end design automation process. Visit **Accellera.org**.

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Sponsored Tutorial

1,20,000 INR *(8 available)*

Tutorials will be held on Thursday. This opportunity includes:

- A 90-minute technical tutorial prepared and presented by your company
- Your company logo will be displayed on the event venue (stage backdrop)
- Your company logo will be displayed on the conference website
- Includes 2 free registrations for speakers
- Copy of the Sponsored Tutorial Attendee List (email addresses included)
- Your company mentioned in the opening session presentation slides

Note: Tutorials will be reviewed and approved by the program committee with respect to technical depth and applicability. In case of multiple organizations coming together for a tutorial only 1 organization would get the sponsorship benefits mentioned above.

Tutorial Deadlines

May 19, 2017	Tutorial Proposals due. Submit at **DVCon-India.org**
June 27, 2017	Accept/Reject Notification
July 7, 2017	All tutorial content due for Conference Program and website: tutorial title, abstract, speaker names, affiliations, and biographies
August 7, 2017	Draft Presentation slides due
September 1, 2017	Final presentation slides due. Presentation slides will be distributed to the attendees in electronic format. Hard copies will not be provided

Call for Tutorials — ESL Track

DVCon India solicits detailed proposals for tutorials that are highly technical and reflect real life experiences in using languages, standards, methods and Electronic Design Automation (EDA) tools. The ESL track aims to accelerate the adoption of SystemC in the Semiconductor Industry. It provides a platform for the SystemC beginners, SystemC/TLM experts, ESL managers and ESL vendors to share their knowledge, experiences & best practices about SystemC usage. Submissions are encouraged in (but not restricted to) the following topics:

- SystemC Language Standards
  - SystemC
  - TLM 2.0
- Virtual-Platforms and System-Level Design
  - Transaction-level modeling for system-level design
  - Hardware/software/embedded co-design
  - System-level design techniques, flows and methodologies
  - High-level synthesis from ESL languages
- Power
  - Low power design
  - Power estimation techniques
  - Power modeling
- Mixed-Signal (AMS)
  - SystemC AMS usage for mixed-signal simulation
  - AMS system-level and concept design

Call for Tutorials — DV Track

In the DV Track we are soliciting detailed proposals for tutorials from industry leaders in the field of Design & Verification. The DV Track provides a platform for the wide Design-Verification community including beginners, intermediate and seniors to learn the latest concepts, techniques, etc. in their respective domains of interest. Submissions are encouraged in (but not restricted to) the following topics:

- UVM – Universal Verification Methodology
- Latest language developments in SystemVerilog including:
  - New and enhanced constructs
  - Assertion enhancements
- Advanced stimulus generation methods, reuse of stimulus across levels of verification (Portable Stimulus)
- Formal verification
  - Coding styles, techniques for assertions for formal
  - Model Checking techniques, target designs/blocks
- Compliance and requirements-driven verification such as DO-254 and IS0 26262 standards
- Debug automation through transaction-level debug, smart tricks to handle performance issues, faster time to debug techniques
- Low Power intent verification through standards such as UPF and related technologies
- Use of IPXACT, SystemRDL in design flow
- Digital and Analog Mixed Signal (AMS) techniques
- Emulation, acceleration, prototyping

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Tutorial Proposal Requirements
Deadline: May 19, 2017

Submit proposals beginning **April 10** at **DVCon-India.org**. Tutorials are 90-minute sessions. DVCon India attendees have the opportunity to learn about different topics during the sessions. A tutorial may have a single speaker or several speakers. In either case, the submitter is responsible for organizing the tutorial. Multiple companies can join together to sponsor a tutorial. If you are interested in providing a tutorial session, please submit your proposal by **May 19, 2017** using the online form available on **April 10**. By submitting the tutorial proposal, you agree to become the tutorial sponsor. The following will be required in order to submit a proposal:

- Title
- Abstract (as would appear in the Conference Program)
- Name, affiliation, phone number and email addresses for all speakers, as well as the titles of any individual presentations, if applicable
- An introduction that specifies the context and motivation of the tutorial submission
- A summary of the specific content of your tutorial and your intended audience, as well as a short paragraph description of each presentation
- Must be descriptive enough to see what this tutorial will address and what the attendees would learn from it
- Provide enough details so that the Tutorial Chairs can evaluate the potential quality and interest of your possible tutorial at DVCon India

Tutorial Roles

Organizer Responbilities

For their tutorial, the Organizer coordinates all tutorial activities with DVCon India, including ensuring that content is delivered in a timely manner and that the final presentation goes smoothly; follow-through is critical, the Organizer must interact with the Conference Coordinator (contact: Trevor Kearns at `trevor@mpassociates.com`):

- The Organizer writes the proposal for the tutorial and the abstract that is submitted for proposal evaluation
- The Organizer selects and confirms the participation of the Presenter(s) (who could include the Organizer)
- The Organizer writes the material that will be included in the website and publications. It is very important that the Organizer write the material to help a potential attendee decide if they should attend this tutorial
- The program material should describe the target audience and their expected level of familiarity with the topic (Expert/Intermediate/Beginner)
- An Organizer can propose multiple tutorials on aligned topics with different speakers

Presenter Responsibilities

The Presenter is responsible for registering for the conference and delivering the presentation.

Questions? Feel free to contact Trevor Kearns at trevor@mpassociates.com for questions on the proposal process.
DVCon India reserves the right to restructure all tutorial proposals.

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