2015 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION INDIA

Sept 10-11, 2015
Leela Palace, Bangalore



# Call for Papers

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**Call for papers is now closed.**

**Important dates:**

- **July 15:** Abstract submission deadline (closed)
- **July 31:** Paper accept/reject notification
- **August 22:** Final paper + PPT/PDF due
- **September 10-11 (Thur-Fri):** DVCon India conference

The **Design and Verification Conference & Exhibition India (DVCon India)** is a highly technical conference in India targeting the application of standardized languages and methodologies for the design and verification of electronic systems, embedded systems and integrated circuits. Hosted by Accellera Systems Initiative, the format of D India is similar to the successful DVCon United States conference held for over 10 years in the Silicon Valley.

The ultimate goal of DVCon India is to boost the interest, usage and development of electronic system designs. We look forward to users sharing the various challenges a solutions adopted by various teams across the industry. DVCon India also provides a much-needed platform to promote upcoming Electronic Design Automation (EDA) an Intellectual Property (IP) standards in India. This highly technical 2-day conference is organized to invite industry experts to learn and share best practices on:

- Modeling, Design and Verification of complex electronic systems at different levels of abstraction such as Virtual prototyping, Architectural Modeling, RTL, Emulation, H acceleration, etc.
- The application of system-level design and verification languages such as SystemC and SystemVerilog
- Virtual Platform for Embedded Software Development
- Novel application of standard Design & Verification languages such as SystemVerilog, PSL, *e*, VHDL, etc.
- SoC Design Verification using the latest trends and methodologies such as UVM-SystemC, graph-based techniques, portable stimulus across block-subsystem-system way up to Post-Silicon
- Architectural Exploration at the early stage and High-level Synthesis
- The use of SystemVerilog Assertions (SVA), PSL and Formal Verification (Model Checking)
- Adoption of Universal Verification Methodology (UVM)
- Leveraging on legacy methodologies based on OVM, VMM and migration to UVM
- IP reuse, design automation and integration standards based on IP-XACT and SystemRDL
- Low-power design and verification using the Unified Power Format (UPF)

General topic areas on Electronic System Level (ESL), Virtual Platform, Verification & Validation, Analog/Mixed-Signal, IP reuse, Design Automation, and Low-power desig verification will be highlighted in tutorials, papers, and poster sessions.

Conference attendees are primarily designers of embedded systems, electronic systems, ASICs and FPGAs, as well as those involved in the research, development and application of EDA tools and IP integration solutions. The DVCon India conference attracts a highly skilled user base active in various industries focusing on research and development of automotive, aerospace, consumer, and wired and wireless communication products.

# Call for Papers - ESL Track

DVCon India solicits presentations that are highly technical and reflect real life experiences in using languages, standards, methods and Electronic Design Automation (ED tools.

The ESL track aims to accelerate the adoption of SystemC in the Semiconductor Industry. It provides a platform for the SystemC beginners, SystemC/TLM experts, ESL managers and ESL vendors to share their knowledge, experiences & best practices about SystemC usage. Submissions are encouraged in (but not restricted to) the follow topics:

- Transaction-level modeling for system-level design (VP, Multi-core, Performance, etc.)
- SystemC Language Development

- Verification Techniques using SystemC-UVM and VPI/PLI, DPI Interface
- Mixed-language environments involving SystemC and SystemVerilog/UVM
- SystemC Analog/Mixed-Signal Extensions & Power Modeling
- High-level synthesis from ESL languages SystemC/C++
- System-level design techniques, flows and methodologies
- Hardware/software/embedded co-design for early development
- HW/SW Co-Simulation and SoC Architecture Exploration
- Debugging Techniques and Configuration and Control in Platform Design

# Call for Papers - DV Track

DVCon India solicits presentations that are highly technical and reflect real life experiences in using languages, standards, methods and Electronic Design Automation (ED tools.

In the DV Track we are soliciting detailed abstracts from industry leaders to share their ideas, thoughts and experiences in solving some of the most complex challenges ir respective fields of work/research. This track provides a platform for the wide Design-Verification community including beginners, architects/experts, managers and EDA v to share their knowledge, experiences and best practices about Design-Verification. Submissions are encouraged in (but not restricted to) the following topics:

- Using multiple HDLs and/or HVLs in a design cycle
- Novel application of existing standard DV (Design-Verification) languages such as SystemVerilog, PSL, *e*, VHDL, etc.
- Latest language developments in SystemVerilog
- Advanced stimulus generation methods, reuse of stimulus across levels of verification (portable stimulus)
- System-on-Chip Verification approaches to handle complexity, performance and reusability requirements
- Adoption of UVM
- Advanced techniques/features and extensions to UVM
- Real life applications of assertions using SVA and/or PSL
- Formal and semi-formal techniques, Assertion automation/synthesis
- Verification process and resource management
- Compliance and requirements-driven verification such as DO-254 standards
- Debug automation through transaction-level debug, smart tricks to handle performance issues, faster time to debug techniques
- Low Power intent verification through standards such as UPF and related technologies
- Usage of IPXACT and SystemRDL in design flow

- AMS challenges in Verification, usage of custom extensions to UVM/SystemVerilog to handle AMS related complexities

# Submission Guidelines

Submit Abstract

Submit abstracts at: **www.easychair.org/conferences/?conf=dvconindia2015**

**To spare you the many hours of preparation associated with other paper submissions, DVCon India has the following process:**

- Submit a 500-1000 word abstract highlighting what you wish to present at DVCon India. The program committee will evaluate your abstract. The deadline for abstract s is **Wednesday, July 15** (closed).
- Authors of exceptionally strong abstracts will be shortlisted for oral or poster presentation at the conference. They will present their work at DVCon India on Thursday, S 10 or Friday, September 11.
- Consistent with the requirements for other DVCon presentations, ***your presentation may contain your company logo only on the title slide***.

**An abstract is expected to include the following details:**

1. A title
2. Name, affiliation, phone number and email addresses for all authors.
3. An introduction that specifies the context and motivation of the submission.
4. A summary of the specific contributions of your work.
5. A summary that highlights results. To evaluate your contribution, you must specify some results.
6. References, if appropriate

Your abstract can be at most two pages. You can format it in single or double column. Provide enough details so that the Technical Program Committee can evaluate the potential quality and interest of your possible presentation at DVCon India. **A one-paragraph summary will not fulfill this requirement.**

**Download abstract submission template**

**View/download 2014 conference proceedings**

# Questions?

Feel free to **contact the Technical Program Committee** for questions on the submission process.

## Conference program

**September 10-11, 2015**
Tutorials and exhibition

## Conference venue

The Leela Palace Bangalore
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