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COMMUNITY NEWSLETTER & UPCOMING EVENTS

Special DVCon India Newsletter: July 2015

IN THIS ISSUE:

2015 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION INDIA

Sept 10-11, 2015
Bangalore, India

Message from the Technical Program Chairs

Last year saw the debut of the Design and Verification Conference and Exhibition (DVCon) India and the event was a great success. We are delighted to let you know that DVCon India will return this year, September 10-11 at the Leela Palace in Bangalore. The combination of a strong technical conference and an exhibition hall with leading EDA vendors makes this a must-attend show for designers, verification engineers, and system-on-chip (SoC) project managers.

Sponsored by Accellera Systems Initiative, the conference provides multiple opportunities to interact with industry experts delivering keynote speeches, invited talks, tutorials, panel discussions, technical paper presentations, poster sessions, and exhibits. Attendees will also get the latest information on numerous Accellera standards for system design, modelling, and verification. These standards include UVM, SystemC (and variants such as SystemC-AMS, SCV, CCI, and the synthesis subset), SystemVerilog, PSL, AMS assertions and coverage, Verilog, IP-XACT, OCP, UPF, and many more.

The 2-day event will be attended by industry leaders, system architects, verification experts, SoC integrators, chip designers, IP developers, VIP developers, and firmware engineers. The conference has two parallel tracks:

- Electronic System Level (ESL), including virtual prototypes of electronic systems and SoCs, pre-silicon software development and debug, power and performance analysis with realistic use cases, architectural exploration, high-level synthesis, and interoperability standards for system models
- Design and Verification (DV), including design and verification languages, simulation methodologies based on SystemVerilog, including the Universal Verification Methodology (UVM), and complementary technologies such as formal verification, hardware acceleration, in-circuit emulation (ICE), and prototyping

DVCon India is a unique opportunity to share your work, experience, and methodologies with the broader community. We are looking for high-quality **paper** and **tutorial** abstract submissions from the engineering community in industry and academia providing insights into the work to be presented at the conference. We expect abstracts to provide a clear description of the work or methodology along with relevant data to support the submission. We also encourage authors to explain the impact to their business and how this work is relevant to the broader industry. The deadline for abstracts is extended to **July 15, 2015**, so please be timely with your submissions.

Thanks, and we hope to see you all at DVCon India!

Saurabh Tiwari, Intel
ESL Track Technical Program Committee Chair

Srinivasan Venkataramanan, CVC
DV Track Technical Program Committee Chair

Industry Drivers for ESL Track

Systems and SoCs are growing ever larger and more complex. The traditional simulation testbenches running an RTL representation of the design are reaching their limits of speed and capacity. Many SoC teams have moved their focus to higher-level representations of the design, typically using SystemC models. Two key aspects of ESL-based development are driving industry innovation. The first is the use of highly efficient virtual platforms to simulate the high-level models for both verification and performance assessment. The second is the use of high-level synthesis to use the SystemC models as the golden design source and to generate RTL and low-level models from them. We encourage abstracts for the ESL Track reflecting these two trends. Specific suggested topics include:

- Transaction-level modeling of systems and SoC
- Verification techniques using SystemC-UVM or other C/C++ testbenches
- High-level synthesis techniques to reduce power and increase performance
- Hardware-software co-development and co-verification
- Links between ESL and embedded systems software
- ESL extensions to handle modeling and verification of analog/mixed-signal (AMS) designs

Industry Drivers for DV Track

Although UVM has been very successful on many SoC projects, verification teams are starting to hit a wall. Some teams perform very little simulation of the complete design, relying on hardware platforms such as ICE or FPGA prototypes. In addition to this move to hardware earlier in the project, two other trends are clear. The first is reliance on static methods such as formal analysis and advanced lint tools rather than simulation to find a wide class of design bugs. In addition, software-driven verification and other forms of portable stimulus are gaining in importance, including an Accellera working group working on standardization in this area. Abstracts reflecting these three trends are especially welcome. Specific suggested topics include:

- Multi-language and other extensions to UVM
- Management of verification process, resources, and metrics
- Formal techniques, assertion automation/synthesis, and static verification
- Software-driven verification using C/C++ embedded test cases
- Debug automation, including identification of error sources
- DV extensions to handle verification of analog/mixed-signal (AMS) designs

Industry Drivers for DVCon India

The semiconductor industry has been transformed in the shift from industrial computation to consumer electronics, and this transformation will continue with automotive electronics, wearables, and other Internet-of-things (IoT) applications. Low-power design techniques and power management will continue to be a key area of focus. Security and privacy become more important every day given the sensitive nature of data available from IoT devices. New standards for reliable design and verification are likely to emerge, and EDA tools must ensure conformance. Abstracts on forward-looking topics that span multiple areas of SoC development will be evaluated highly. Specific suggested topics include:

- Performance and power management techniques across the entire development cycle
- Design and verification methodologies for privacy and security of IoT devices
- Compliance- and requirements-driven verification, including the DO-254 standard
- Emerging standards and new requirements for advanced automotive applications

Highlights from DVCon 2014

In 2014, the first DVCon India was held in Bangalore. Two parallel tracks were identified for the conference—"Design and Verification (DV)" and "Electronic System Level (ESL)"—based on the experience gained from the Indian SystemC Group, sponsorship from Accellera and DVCon US. Though we started small in March 2014 with only a few people, we progressed to become a well-developed and strong team with leaders from many different companies collaborating voluntarily and working towards the event's success. There was an overwhelming response at each stage right from the call for abstracts. Every abstract and tutorial proposal was reviewed by more than three members and finalized for selection after internal discussion. The Technical Program Committee welcomed thoughts from the authors on their papers and made it flexible for them to present in a style that would reach the audience better.

The two-day event was inaugurated with a lamp-lighting ceremony and welcome note by the Chair of DVCon India 2014. Dr. Walden C. Rhines, CEO of Mentor Graphics, Dr. Mahesh Mehendale, CTO, MCU at Texas Instruments, Janick Bergeron, Synopsys Verification Fellow, and Mr. Vishwas Vaidya—AGM, Electronics at Tata Motors, delivered the key speeches. DVCon India 2014's main stage played host to the keynote presentations, opening ceremonies, and best paper and poster awards. Many different types of sessions were conducted as part of the event on both the days, including invited talks, invited tutorials, technical paper presentations, poster sessions and panel discussions on the latest trends in the industry. Again, the response was mind-blowing!

Initial expectations were that a small number of delegates would attend, but DVCon India 2014 managed to bring together over 450 attendees from more than 80 different companies and universities. Feedback from attendees on the two-day event, especially on the technical program, was very encouraging and positive. We expect the 2015 conference to be a huge success given the strong content and the strenuous efforts put in by the planning team. Here are two pictures taken during the event last year:

www.dvcon-india.org