2015 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION INDIA
Sept 10-11, 2015
Leela Palace, Bangalore

Conference Sponsor
accellera SYSTEMS INITIATIVE™

DVCon India Newsletter: August 2015

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Message from the General Chair

DVCon is an excellent platform promoted by Accellera Systems Initiative to bring together the engineering community focused around system-level, SoC-level and IP-level design and verification. DVCon India is an extension to the highly successful DVCon US event. With growing design complexity there is a clear need for both design and verification reuse. Having standards used by all participants of the ecosystem is the right way forward. Accellera has been instrumental

in defining, developing and driving the adoption of standards. DVCon is a clear reflection of the work done throughout the year by the community in many different parts of the world.

Last year the debut of DVCon India witnessed more than 450 participants representing more than 80 different organizations. This year, we expect DVCon India to be even bigger and better. It will be hosted on September 10-11 at Leela Palace in Bangalore. The committee has worked tirelessly to put together a 2-day power-packed schedule with keynotes, panels, industry talks, tutorials, papers, posters, an exhibition and a Gala dinner. The conference has two parallel tracks:

- Electronic System Level (ESL), including virtual prototypes, pre-silicon software development and debug, power and performance analysis, architectural exploration and high-level synthesis
- Design and Verification (DV), including simulation methodologies, static design analysis, formal verification, hardware acceleration, in-circuit emulation (ICE) and silicon prototyping

Participants are strongly encouraged to **review the entire program** and attend sessions of interest from both tracks. We thank everyone who has contributed and look forward to a successful event. DVCon India rightly promotes the 4 Cs: connect, contribute, collaborate and celebrate. Come join us!

Thanks, and we hope to see you all at DVCon India!

Gaurav Jalan, Smartplay
Steering Committee General Chair

Who Should Attend DVCon

DVCon events attract a wide range of attendees from all types of electronics companies. Hardware designers will find out about the latest IP and SoC design techniques, including the ongoing industry migration from RTL to high-level synthesis. Verification engineers will learn about the latest extensions to the Universal Verification Methodology (UVM) and supplemental techniques to traditional simulation testbenches. Architects will discover high-level modeling techniques to accurately predict power consumption and system performance early in the development process. Technology managers at every level will hear how other companies are accelerating their projects while maintaining or even improving product quality. DVCon India is a practical conference with information that attendees can use as soon as they return to their offices. With 65 sessions across two days, there is something for everyone.

Gala Dinner and Accellera Celebration

One exciting addition to the DVCon India program this year is a Gala dinner on Thursday evening. This event celebrates two important milestones. First, this year is the tenth anniversary of the standardization of SystemVerilog, originally developed within Accellera Systems Initiative, as IEEE Standard 1800-2005. Combining advanced design constructs, constrained-random testbench support, functional coverage metrics and assertions into a single language was a major technical accomplishment. The great success of SystemVerilog shows its power as well as its ease of use.

The second milestone is the transfer of the Universal Verification Methodology (UVM) to IEEE for standardization. Developed within Accellera and first released in 2011, UVM builds on SystemVerilog to define a uniform way to develop flexible and reusable testbenches for hardware verification. IEEE has formed the P1800.2 working group to standardize UVM. In addition to the celebration of these two milestones, the Gala dinner will feature entertainment

and will offer extra time for networking and relaxing after a busy day of technical sessions.

A Few of the Don't-Miss Sessions

For an overview of the DVCon India technical program, view our **program-at-a-glance**. With 65 sessions, there are many highlights that we could discuss. However, we want to make a special note of the 10 tutorials, four keynote talks, and three technical panels on the program. Tutorials offer the chance to dig deeply into a single topic or several related topics in a 90-minute session. The subjects to be covered this year include:

- Leveraging Portable Stimulus across Domains and Disciplines
- Software Driven Verification at SoC Level
- Expediting the Code Coverage Closure Using Static Formal Techniques – A Proven Approach at Block and SoC Levels
- FPGA Implementation Validation and Debug
- Early Architecture Exploration leveraging TLM2.0: Challenges & Opportunity
- Creating SystemVerilog UVM Testbenches for Simulation and Emulation Platform Portability to Boost Block-to-System Verification Productivity
- Addressing SOC/IP Verification Framework Creation with UVM Centric Mechanisms
- Advanced Debug for SoC Verification

Keynote speakers include:

- **Harry Foster**, Chief Scientist, Design Verification Technology Division, Mentor Graphics
- **Manoj Gandhi**, Executive Vice President and General Manager, Verification Group, Synopsys
- **Vinay Shenoy**, Managing Director, Infineon Technologies India Pvt. Ltd

Panels are ideal conference sessions because they offer two benefits. First, attendees get to hear from the industry's foremost experts on topics of critical importance. Second, the audience can participate directly in the session by asking the panelists questions from the floor. This year's DVCon India features three panels certain to draw crowds of curious engineers:

- Supporting the Evolving Verification Flow
- IoT Verification: Cubbon Park or Jurassic Park

- Electronic System Level (ESL)

Vendor Exhibition

The technical sessions at DVCon India will present dozens of new ideas, applications and methodologies to help design and verification engineers do their jobs better and faster. In many cases, commercial solutions can help accelerate the adoption of these new approaches. More than 30 vendors will participate in the DVCon exhibition, staffing their booths with knowledgeable personnel offering discussions and demonstrations of their products.

Register to Join in the Fun!

The first DVCon India was held last year in Bangalore, with the same two parallel DV and ESL tracks offered this year. Feedback from attendees was very positive. They found the technical sessions intellectually stimulating, but with a practical aspect that allowed knowledge gleaned at the conference to be applied in their everyday jobs. With even more sessions this year, the committees organizing the event have every expectation that it will be even more successful and offer even more valuable information on modern design and verification.

But beyond the technical benefits, last year's attendees found DVCon India to be fun. The sessions were lively, not dry academic papers. The panels stirred up controversy and invited audience participation. There was also plenty of time for networking with friends, colleagues, competitors and exhibition vendors. This year the time for networking has been increased, including the addition of the Gala dinner. So don't miss out on this once-a-year event. **Registration is now open!** See you at Leela Palace in September!

Are you interested in becoming a Conference Sponsor? **Contact us!**

www.dvcon-india.org