2015 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION INDIA

Sept 10-11, 2015
Leela Palace, Bangalore

Conference Sponsor
accellera SYSTEMS INITIATIVE™

DVCon India Newsletter: September 2015

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General Update & Keynote Speakers

This is the third and final newsletter in our series leading up to the DVCon India conference. We first notified you about the event and issued a call for papers, panels and tutorials. In the last newsletter we discussed some of the highlights from the initial program. Now the entire technical program has been finalized and **published**. We'd like to devote this final issue to covering some of the sessions of particular interest from both tracks, Electronic System Level (ESL) and Design and Verification (DV), as well as Keynote Speakers.

We'll also remind you about the vendor exhibition and the special Gala dinner on Thursday evening. The conference will be September 10-11 at Leela Palace in Bangalore. Please plan to attend, and please spread the word to your friends, family, neighbors, colleagues and even competitors. All are most welcome, and we look forward to seeing you there.

Day 1: September 10th starts with a Keynote speech by our Gold Sponsor Mentor Graphics titled "**From Growing Complexity to Faster Horses**." Harry Foster, Chief Scientist of the Design Verification Technology Division will discuss the rising complexity throughout the entire design ecosystem—from many small, yet intricately connected devices all the way through very large, highly integrated, multicore SoCs designs.

Day 2: September 11th starts with a Keynote speech from our Gold Sponsor Synopsys titled “**Propelling the Next Generation of Verification Innovation**." Manoj Gandhi, VP & GM of the Verification Group, will highlight the major drivers that have led the evolution of verification and how these drivers, new market dynamics, and increasing complexities are impacting the future of verification technology innovation.

The other two invited keynote speakers will target their speeches towards the **"Make in India"** Initiative.

On September 10th, Vinay Shenoy, Managing Director of Infineon Technologies India will deliver a speech on the highly emphasized "**Make in India" Implies Innovate-Engineer-Manufacture**." Mr. Vinay will highlight the various initiatives to develop technical competence along the entire electronics value chain, promote start-ups, and provide access to locally made products in government purchases.

On September 11th, Atul Bhatia, Mentor & Angel Investor will deliver a speech on “**Opportunities for Semiconductor Design Startups in India**." Mr. Atul will speak about the challenges and how to support in an ecosystem for small and medium sized companies that focus in the area of B2B markets for technology-driven products.

Update: Highlights in the ESL Track

An overview of the DVCon India technical program is available here: **dvcon-india.org/conf/program-at-a-glance**. The ESL track alone has 12 talks and three posters covering a wide range of system-level topics. The two leading standards in the ESL space—SystemC and transaction-level modeling (TLM)—will be addressed in multiple sessions. Virtual platforms and virtual prototypes are everywhere these days, and the DVCon India program reflects their popularity with four talks. There are presentations related to specific types of designs, including CPUs and memory subsystems. Topics go beyond simulation into emulation and automated chip testing. One session on testing drivers even moves from the hardware design and verification domain to the software world.

Finally, don’t forget the panel on "**The ESL Continuum**" and the five tutorials we discussed in the last newsletter. Note that the tutorial "**Leveraging Portable Stimulus across Domains and Discipline**" will be of high interest to those in the DV track as well as the ESL track. You can switch back and forth between tracks whenever you like.

Update: Highlights in the DV Track

The details for the sessions in the DV track are also available here: **dvcon-india.org/conf/program-at-a-glance**. The DV track drew tremendous interest in the call for papers, with 27 talks and 11 posters accepted. The most popular topic is the Universal Verification Methodology (UVM) standard. Related talks include efficient use of the UVM register layer, linking the UVM to hardware platforms, the art of writing UVM predictors, the specifics of verifying processors and extending the UVM to analog/mixed-signal (AMS) designs. The topics go beyond simulation testbenches to include:

- Effective use of acceleration, emulation and FPGA prototyping
- Automatic generation of constraints for clock domain crossing (CDC) checks
- The latest advances in assertion-based verification (ABV) and formal analysis
- Verification of static timing analysis (STA) constraints

Several sessions include talks on the most leading-edge methodologies, including graph-based verification, software-driven verification, automated coverage closure and power-aware simulation. As mentioned in the last newsletter, the DV track also features six tutorials and two panels. The Internet of Things (IoT) is one of the hottest topics in all of electronics, and the panel "**IoT Verification: Cubbon Park or Jurassic Park**" is sure to be popular with attendees from both tracks. Again, you can switch back and forth between tracks whenever you like.

Reminder: Gala Dinner and Accellera Celebration

One exciting addition to the DVCon India program this year is a Gala dinner on Thursday evening. This event celebrates two important milestones. First, this year is the tenth anniversary of the standardization of SystemVerilog, originally developed within Accellera Systems Initiative, as IEEE Standard 1800-2005. Combining advanced design constructs, constrained-random testbench support, functional coverage metrics and assertions into a single language was a major technical accomplishment. The great success of SystemVerilog shows its power as well as its ease of use.

The second milestone is the transfer of the Universal Verification Methodology (UVM) to IEEE for standardization. Developed within Accellera and first released in 2011, the UVM builds on SystemVerilog to define a uniform way to develop flexible and reusable testbenches for hardware verification. IEEE has formed the P1800.2 working group to standardize the UVM. In addition to the celebration of these two milestones, the Gala dinner will feature entertainment and will offer extra time for networking and relaxing after a busy day of technical sessions.

Reminder: Vendor Exhibition

The technical sessions at DVCon India will present dozens of new ideas, applications and methodologies to help design and verification engineers do their jobs better and faster. In many cases, commercial solutions can help accelerate the adoption of these new approaches. **See which vendors** will participate in the DVCon exhibition, staffing their booths with knowledgeable personnel offering discussions and demonstrations of their products.

Portable Stimulus Birds-of-a-Feather

Portable stimulus is a hot topic in the industry, with Cadence, Mentor Graphics and Breker announcing a joint contribution to Accellera's Portable Stimulus Working Group (PSWG) to help develop a standard. This informal breakfast session on September 11 from 8:00-8:45 offers the chance for engineers to ask questions about this contribution and provide feedback on what they would like to see in the standard. Several members of the PSWG will be present to listen and share their thoughts.

Register to Join in the Fun!

DVCon India will be a unique mix of intense technical education, lively interaction sessions and networking fun. Every successful aspect of last year's inaugural event has been expanded this year for an ever bigger and better show. Don't miss out on your chance to participate; there are only a few days left to register. Please visit **dvcon-india.org/conf/registration**. We will see you at Leela Palace soon!

www.dvcon-india.org

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