Opening Talks and Lamp Lighting Ceremony

Time: 9:30am - 9:45am | Room: Grand Ballroom

Join us for the opening session of the 2016 Design and Verification Conference and Exhibition India, featuring the lamp lighting ceremony.

Keynote - Design Verification: Challenging Yesterday, Today and Tomorrow

Time: 9:45am - 10:30am | Room: Grand Ballroom

Design verification methodologies are in a endless race to catch up with exploding verification needs. As soon as the verification industry standardizes on a methodology, a new set of requirements emerges. Dr. Rhines will review the major phases of the verification evolution over the past several decades and then focus on the challenges of newly emerging problems. Functional verification still is a primary concern, but new requirements for security and safety are becoming more important and could ultimately pose challenges more daunting than those we have faced in the past.

Biography:

Walden C. Rhines is Chairman and Chief Executive Officer of Mentor Graphics, a leader in worldwide electronic design automation with revenue of $1.24 billion in 2014. During his tenure at Mentor Graphics, revenue has nearly quadrupled and Mentor has grown the industry's number one market share solutions in three of the ten largest product segments of the EDA industry.

Prior to joining Mentor Graphics, Rhines was Executive Vice President of Texas Instruments' Semiconductor Group, sharing responsibility for TI's Components Sector, and having direct responsibility for the entire semiconductor business with more than $5 billion of revenue and over 30,000 people.

During his 21 years at TI, Rhines managed TI's thrust into digital signal processing and supervised that business from inception with the TMS 320 family of DSP's through growth to become the cornerstone of TI's semiconductor technology. He also supervised the development of the first TI speech synthesis devices (used in "Speak & Spell") and is co-inventor of the GaN blue-violet light emitting diode (now important for DVD players and low energy lighting). He was President of TI's Data Systems Group and held numerous other semiconductor executive management positions.

Rhines has served five terms as Chairman of the Electronic Design Automation Consortium and is currently serving as a director. He is also a board member of the Semiconductor Research Corporation and First Growth Family & Children Charities. He has previously served as chairman of the Semiconductor Technical Advisory Committee of the Department of Commerce and as a board member of the Computer and Business Equipment Manufacturers' Association (CBEMA), SEMI-Sematech/SISA, Electronic Design Automation Consortium (EDAC), University of Michigan National Advisory Council, Lewis and Clark College and SEMATECH.

Dr. Rhines holds a Bachelor of Science degree in metallurgical engineering from the University of Michigan, a Master of Science and Ph.D. in materials science and engineering from Stanford University, a master of business administration from Southern Methodist University and an Honorary Doctor of Technology degree from Nottingham Trent University.

Speakers:

Walden Rhines - *Mentor Graphics Corp.*

Thank You to Our Sponsor: Mentor Graphics®

Invited Keynote - A Make in India Roadmap for Systems Engineering by RISE Group, IIT Madras

Time: 10:30am - 11:00am | Room: Grand Ballroom

Government of India has begun a major drive for "Make in India" initiative. There are many major drives of this initiative on electronic systems. Needless to say that computation and communication are the critical and primary areas where electronic systems are deployed. The work at RISE LAB-IIT-Madras keeping the broad picture in Mind has come up with a Secure Computation and Communication frame work. The frame work and its components are envisaged designed developed and tested at RISE LAB CSE Department IIT Madras, thus making it a true 'Make in India Initiative'.

The existing systems which are available have following short falls:

- They are commercially off the shelf solutions offered by Foreign Vendors.
- Possible presence of NoWn Verifiable Trojans and Malwares.
- Not truly "End to End' Secured

Our Focus or work consists of the following:

1. A complete end to end secured communication and compute system frame work with the following components.
- Secure I.M.P (Shakti) Processor Family.
- S.C.I.O.N (Scalability Control and Isolation on Next generation Networks) Framework
- Secured Tablet
- Secured Network Switch
- Secured Network Router
- Secure IOT End device
- Secure NAVIC/IRNSS (Anti-Jam) Hand Held Receivers

2. A testing frame work for potential reverse engineering of the above system using Side Channel analysis.

3. A verification frame work for Security of Cryptographic Implementations in the above systems.

Relevance to the Nation's SECURITY and DEFENSE:
The proposed secured systems along with testing and verification framework offer the following unique advantages which highlights its relevance.

- Indigenously developed End to End security in a typical communication network.
- Difficult to reverse engineer the system and its components.
- Formal certification of cryptographic implementation to overcome.
  - Lack of complete control over design components and the product features to suit specific needs of Defense and other strategic establishments.
  - Lack of End to End Security at the end device hardware plane.

The Team

Faculty
- Professor V. Kamakoti
- Professor Balaraman Ravindran
- Professor Chester Rebeiro
- Professor Aritra Hazra

Consultants and Researchers
- G S Madhusudan
- Dr M.J.ShankarRaman
- V.S Vasan
- K.S.Venkataraghavan
- Aspiring young minds @ IIT-M

Speakers:

Kamakoti Veezhinathan - *Indian Institute of Technology Madras*

Biography: Professor KamaKoti also fondly known as Kama amongst his students, in the professional and teaching community is a Senior Professor at CSE Department IIT Madras. Kama finished his Bachelor of Computer Science and engineering, from Sri Venkateshwara College of Engineering in 1989 and moved on to do his Master of Science by research from IIT Madras in 1991. He then finished his Doctor of Philosophy in IIT Madras in 1995. Kama continued his thirst and quest for knowledge by doing his Post-doctoral fellow ship in Institute of Mathematical science, Chennai and as a Research Associate at the Supercomputer Education and Research Centre, IISC Bangalore. Kama had a brief stint of Industrial experience prior joining to IIT Madras in 2001 at ATI research Silicon Valley Inc. for two years. He then moved back to the academia in 2001, joined as an Assistant Professor in CSE Department IIT Madras.

In these 16 years in academia, Kama and his students have published numerous IEEE, IET ACM journals. Kama has guided nine PHD students and at present is guiding 9 more. These areas have been varying from VLSI, Security, and Networking etc. Kama is one of the coordinators of IMPRINT Program the first of its kind MHRD supported Pan-IIT + IISc joint initiative. IMPRINT programs aims to address the major science and engineering challenges that India must address and champion to enable, empower and embolden the nation for inclusive growth and self-reliance. He coordinates the security and defense domain of the IMPRINT Program. Kama's prowess doesn't stop at being an excellent academician, he is a well-known Carnatic music enthusiast, a sustainable organic farming enthusiast. He runs his own different kind of "go-shAlA, housing feeding and protecting old and non-milking cows.

Kama also serves as a Director in charge of technical operations of City Union Bank, one of the leading private bank with its headquarters in Kumbakonam, Tamilnadu. Though to his hat Prof Kama has had many feathers added, the most prominent among them are Young Faculty Recognition Award" for the year 2007 in April 2007 and DRDO Academic Excellence Award instituted by DRDO in recognition of the contribution from Academicians to various programs of DRDO. This award was given by Hon'ble Prime Minister Shri. Narendra Modi in August 2014.

Tea Break and Exhibits Networking

Time: 11:00am - 11:30am | Room: Pre-Function Area Mezzanine Level

Enjoy a tea break while you mingle with DVCon India's exhibitors, located in hallways throughout the conference area.

ESL Invited Keynote - Microprocessors to Smartphones to Autonomous Cars to Deep Learning

Time: 11:30am - 12:10pm | Room: Royal Ballroom

Since the introduction of 4004 in 1971, the primary driver for all design development and EDA flows around it has been MOSFET miniaturization. Chip designers have strived and streamlined their design in anticipation of an end-application. The winner most often has been the team or the company that anticipates the killer end-application well in advance.

In the 1990s, these end-applications were desktop computing. Resulting in the emergence of multi-core architectures. In the 2000s, these end-applications have been mobile computing. Resulting in breakthroughs on low power, interconnect and memory performance management architectures.

So what will be killer end-application for the next decade? In the last 3 years, visual computing has seen a revolution of sorts. With the shared emergence of Machine Learning and Large Visual datasets, we are witnessing a time where methods such as Deep Learning are outperforming traditional rule-based algorithms. Autonomous cars are one end-application we are witnessing. But that's just a tip of the ice-berg. The possibilities on visual computing driven by Deep Learning technology are immense. If so, then how would it impact the overall system architecture and the ESL flows around it?

This talk will look back at the application/technology/Design Abstraction trends of the last 45+ years, ESL evolution & contribution to design industry and share a few thoughts on how the same might look like in the next decade or so.

Biography:
Subrangshu started his career in 1999 as Member Technical Staff in Hewlett Packard Microprocessor Labs in Fort Collins, Colorado.

After returning back from USA in 2001, he joined Texas Instruments, where he spent more than 13 years developing IPs and SOCs for catalog, wireless, industrial and automotive sectors.His last role in TI was Director, Platform and SOC Development in Processor BU.

In 2014, Subrangshu joined Canon, where he is currently Senior Director & Head of India Systems Development Center (ISDC) - R&D division of Canon India. In ISDC, his team is involved in developing next generation embedded platform solutions across both hardware and software. These solutions are then used across different business groups in Canon. Subrangshu has done his B Tech in Electrical Engineering from IIT Kanpur and MS in Electrical Engineering and Computer Science from University of Michigan, Ann Arbor. He has four patents granted to him and has authored 14 papers including a tutorial in external technical conferences. In his spare time, he can be seen playing badminton and sometimes table tennis.

Speakers:

Subrangshu Das - *Canon India Pvt. Ltd.*

DV Keynote - Verification for Complex SOCs

Time: 11:30am - 12:10pm | Room: Grand Ballroom

Verifying a complex SoC consisting of tens of embedded cores and hundreds of IPs, with complex low power design features is a major challenge in the industry today. The focus of this keynote will be on the challenges and potential solutions for the verification of complex SoCs. Given the size and complexity of modern SoCs, tests can run for 18 - 24 hours or even more. The first challenge is the need for speed and how to get the best verification throughput. Another challenge is how to rapidly develop all the required test benches required for verifying an SoC. The test benches have to be developed in a way which can achieve good performance in both simulation and hardware acceleration. Yet another challenge is how to create all the tests required to stress the SoC under the application use cases, low power scenarios, and multi-core coherency scenarios. The tests have to be developed in a way that they can be reused across pre-silicon and post-silicon verification and validation platforms. One has to figure out how to measure verification coverage across formal, simulation, and acceleration platforms at the SoC level to know when you are done. Finally, there is the challenge of how to effectively debug across RTL, test bench, and embedded software on multiple verification platforms.

Biography:
Alok Jain is a Senior Group Director in the Advanced Verification business unit at Cadence. He is serving as the R&D lead for the simulation performance program. He has a PhD in the area of Formal Verification from Electrical and Computer Engineering from Carnegie Mellon University, USA. He has around 20 years of industry experience. His expertise includes RTL functional verification, gate-level verification, coverage, metric driven verification and formal verification. He has 30+ technical papers in internal and external conferences and 10+ granted patents in the area of RTL simulation, Formal verification and transistor analysis.

Speakers:

Alok Jain - *Cadence Design Systems, Inc.*

Thank You to Our Sponsor: cadence®

ESL Invited Panel: An Entry Level Vehicle for IoT Market Space

Time: 12:10pm - 1:00pm | Room: Royal Ballroom

Moderator:

Dineshkumar Selvaraj - *Infineon Technologies India Pvt. Ltd*

IoT is one of the hottest buzzword in the technology arena and is projected to be the next big wave of technology revolution. ESL has long promised to be an evangelization vehicle for rapid prototyping, early exploration and speedier exploration. The focus of the panel discussion is to present and brainstorm on how the ESL promise can be applied to enable IoT market to foster Innovation and Development to create next generation of market and technology leaders in the industry.

The panel hosts ESL and industry leaders from a spread of domains ranging from ESL vendors to leaders representing end users responsible for designing and defining products and portfolios for the market.

Opening Talks

Time: 9:30am - 9:45am | Room: Grand Ballroom

Join us as we re-open the conference on Friday, looking forward to an interesting schedule of keynotes, an invited tutorial, posters, and the technical paper sessions.

Keynote - Today's SoC Verification Challenges: Mobile and Beyond

Time: 9:45am - 10:30am | Room: Grand Ballroom

With the explosion of the Internet of Things (IoT), consumers are increasingly demanding devices that are faster, smaller and more cutting-edge. As a result, SoC teams are faced with the challenge of how to verify these highly complex chips, while also confronted with time to market pressure and earlier software bring-up. Mr. Gupta will start with an examination of the current complexities in verification and key challenges that SoC teams face today. He will discuss the newest solutions used to address these issues, and their subsequent integration for streamlining overall process flow. The presentation will conclude with a prediction of how these new solutions will impact the future of verification.

Biography:
Sushil Gupta is a Group Director of Engineering in the Verification Group at Synopsys.

In his current role, Sushil is responsible for Synopsys' SpyGlass platform for static analysis. Sushil joined Synopsys in 2015 as part of acquisition of Atrenta. He has 30 years of industry experience which spans various roles in engineering management and leadership in EDA and VLSI Design companies. He started his career at Texas Instruments in 1986 and has worked at Gateway Design Automation, Cadence, Duet Technologies, Motorola SPS and Atrenta.

He is a gold medalist from Delhi College of Engineering where he received a B. E. in Electronics and Communication Engineering.

Speakers:

Sushil Gupta - *Synopsys, Inc.*

Invited Keynote

Time: 10:30am - 11:00am | Room: Grand Ballroom