August 2016 Update

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Message from the Technical Program Chairs

The third edition of DVCon India celebrates the engineering community engaged in the system design and verification fields, and brings them together in an unparalleled event. This year we will celebrate the high level of innovation and community effort that have contributed to the success of numerous Accellera standards, including SystemVerilog, UVM, SystemC, UVM-SystemC, and SystemC-AMS. You will have the chance to hear about the latest developments from both industry and academia, divided into two parallel tracks:

- Electronic System Level (ESL), including virtual prototypes of electronic systems and SoCs, pre-silicon software development and debug, power and performance analysis with realistic use cases, architectural exploration, high-level synthesis, and interoperability standards for system models
- Design and Verification (DV), including design and verification languages, simulation methodologies based on SystemVerilog, including the Universal Verification Methodology (UVM), and complementary technologies such as formal verification, hardware acceleration, in-circuit emulation (ICE), and prototyping

Attendees are free to choose between the ESL and DV tracks based on your topics of interest. You can listen to formal paper presentations or chat informally with the authors in poster sessions. The technical program also offers keynote addresses from industry

leaders, panels on hot ESL and DV topics, and many opportunities to network with your peers. We summarize some of the sessions below; the complete program is now available on the DVCon India site.

On behalf of the entire Technical Program Committee, we would like to thank all those of you who submitted proposals. Many companies stepped up to share their activities, and this year's event also has increased academic participation in terms of committee members, paper submissions and invited talks. The outstanding program would not have been possible without the efforts of many individuals submitting and reviewing the proposals. DVCon India is very aptly hosted by the Technology Capital of India – Bengaluru, which is home to some of the biggest names in the field as well as the emerging startups that aspire to make their mark in the field of design and verification. Bengaluru Swagata!!

Swaminathan Ramachandran
ESL Track Technical Program Committee Chair

Pushkar Naik
DV Track Technical Program Committee Chair

Overview of the Keynote Talks

DVCon India makes a special effort each year to invite keynote speakers from a wide range of sources, including universities, EDA vendors, hardware developers, and industry organizations. This year is no exception; the keynote addresses include:

- Design Verification: Challenging Yesterday, Today and Tomorrow - Mentor Graphics Chairman and CEO Walden Rhines reviews the past verification evolution and focuses on newly emerging problems
- A Make in India Roadmap for Systems Engineering - Professor Kamakoti Veezhinathan of IIT Madras describes the Secure Computation and Communication framework developed at RISE LAB
- Today's SoC Verification Challenges: Mobile and Beyond - Synopsys Group Director of Engineering Sushil Gupta discusses how the explosion in IoT devices will put even more pressure on verification
- Microprocessors to Smartphones to Autonomous Cars to Deep Learning - Subrangshu Das, Senior Director and Head of India Systems Development Center at Canon India Pvt. Ltd., ponders what will be the killer end-application for EDA over the next decade (ESL Track Keynote)
- Verification for Complex SOCs - Alok Jain, Senior Group Director in the Advanced Verification business unit at Cadence, surveys the many verification challenges for today's complex SoC designs (DV Track Keynote)

Overview of the ESL Track

The first day of the two-day conference is focused on tutorials. The ESL track includes:

- Verification Methodology for High-Level Synthesis from C++/SystemC to RTL - deployment of high-level synthesis into mainstream design flows, with verification methodology being the critical piece for keeping the whole edifice together

- Hybrid Solution Combining Hardware Emulation and Virtual Prototyping for Early Software Development - how speed and accuracy goals can be achieved in the shortest possible time using such hybrid development environments
- Shift left – Success Story of Infineon's AURIX Microcontroller - how the various challenges in supporting multiple platforms, changing requirements, functional correctness, cycle accuracy, fault injection, etc. have been tackled while supporting the customers with optimal resource and efforts
- How Portable Stimulus Addresses Key Verification, Test Reuse, and Portability Challenges - portable stimulus challenges such as linking verification to diagnostics and software, portability to every platform, and resource management, including a set of common usage examples that emphasize specific challenges

A special invited panel has been put together to discuss how ESL can provide an entry-level vehicle for the Internet of Things (IoT) marketplace. Panelists will brainstorm on how the ESL promise can be realized in the emerging IoT market.

The second day of the conference is dedicated to posters and papers that showcase the top submissions as evaluated by the ESL Technical Program Committee. Three posters and twelve papers spread across four sessions of three papers each will be presented. The papers are grouped into the following sessions:

- ESL Power and Energy Modeling
- System Level Design Techniques, Flows and Methodologies
- Hardware/Software/Embedded Co-Design For Early Development
- Hardware/Software Co-Simulation and SoC Architecture Evaluation

Finally, Doulos is conducting a special tutorial on "The Definitive Guide to SystemC TLM2.0" that will be very useful to engineers who are just starting or have some experience with transaction level modeling (TLM) methodology.

Overview of the DV Track

The first day of the two-day conference is focused on tutorials. The DV track includes:

- Advanced UVM Coding Techniques - three aspects of UVM coding at an advanced level: run-time phasing, the sequencer, and random stability
- Advanced Validation and Functional Verification Techniques for Complex Low Power System-on-Chips - addressing one of the prime industry challenges: reducing power consumption and the related complexity in verification of these techniques
- It All Starts with Quality Design - novel technologies that make the designers more efficient and help them to increase the quality of their designs, since design is the starting point, and then comes verification
- An Industry Proven UVM Reuse Methodology for Coverage Driven Block Level Verification to Software Driven Chip Level Verification Across Simulation and Emulation - UVM reuse methodology that addresses block to chip to software testing requirements in both simulation and emulation worlds using a single methodology
- Using Portable Stimulus for SoC Verification as Applied on Mobile, Networking, and Server Designs - state-of-the-art solutions to address SoC-level verification challenges and demonstration of a comprehensive SoC verification flow along with case studies and hardware-assisted/software-driven advanced options

- Thinking Ahead - Advanced Verification and Debug Techniques for the Imminent IoT Wave – how IoT chip development faces additional challenges, on top of smaller and faster, in the form of significant mixed-signal functionality, growing software content, reduced power consumption, shorter design cycle, and lower cost that translate to an exponential increase in design and verification complexity

A special panel on “The Future Verification Flow” features industry stalwarts comparing possible paths for future verification flows, focusing on the roles of simulation, emulation, and formal, including their pros, cons, and costs.

The second day of the conference is dedicated to posters and papers representing the best submissions as evaluated by the DV Technical Program Committee. Ten posters and 27 papers spread across nine sessions of three papers each will be presented. The papers are conveniently grouped as:

- 3 sessions on the most popular topic: UVM/SystemVerilog, focusing on current methodological advancements, novel techniques adopted by users for usage, etc.
- Acceleration and co-simulation, dealing with hardware-assisted verification techniques and software usage in verification
- Analog and Mixed-Signal (AMS) and random number modeling, focusing on mixed-signal verification techniques primarily to increase efficiency
- Processor and SoC-based verification challenges and proposed solutions
- ABV/formal/CDC/x-check verification as an alternative or augmentation to the traditional normal dynamic simulation approach
- Low-power complexities and solutions to efficiently handle their verification requirements
- Selected topics in verification based on user demand and expected interest

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