July 2016 Update

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Message from the General Chair

I am pleased to welcome you all to the third edition of DVCon India, planned for 15-16 September 2016 at the Leela Palace Hotel in Bangalore.

DVCon India is a must-attend conference dedicated to design and verification of IPs, SoCs and electronic systems. The conference provides an excellent platform for attendees to discuss, network and contribute to the standards, flows and methodologies enabling silicon product realization. Following many years of success for DVCon in Silicon Valley, the Indian edition of this conference has received overwhelming response for the last two years.

Today, the semiconductor industry is experiencing a major change in its landscape. Post the PC & mobile eras, all eyes are on IoT, an ecosystem of interconnected devices that are high on performance, low on power consumption, cheap and highly customized to end user expectations. This requires a paradigm shift in how we design and verify chips enabling first silicon success faster than ever before. Starting from the concept exploration at the system level and bringing it down to the IPs interconnected on the SoC, DVCon India touches different aspects of design and verification. The discussions and information exchange cover a wide variety of topics, representing the latest developments and future trends in this domain.

The Technical Program Committee has worked relentlessly to come up with a 2 day packed agenda covering keynotes from industry luminaries, tutorials from the gurus, panel discussions with experts, and papers and posters from the fraternity. The conference has two parallel tracks:

• Electronic System Level (ESL), including virtual prototypes of electronic systems and SoCs, pre-silicon software development and debug, power and performance analysis with realistic use cases, architectural exploration, high-level synthesis, and interoperability standards for system models

• Design and Verification (DV), including design and verification languages, simulation methodologies based on SystemVerilog, including the Universal Verification Methodology (UVM), and complementary technologies such as formal verification, hardware acceleration, in-circuit emulation (ICE), and prototyping

Attendees are free to choose between the ESL and DV track based on your topics of interest. Some portions of the technical program are now posted on the DVCon India site and the complete details will be available soon.

You will also learn about current and upcoming commercial solutions from the exhibitor booths. Both days provide multiple opportunities to network and connect with your peers in the industry. The technical sessions are spiced up with lot of fun at the gala dinner on the first evening. DVCon India is a unique conference for all members of the semiconductor ecosystem.

I am looking forward to meeting you and joining hands to connect, contribute and celebrate at DVCon India 2016!

Gaurav Jalan
General Chair

Industry Trends Driving the ESL Track

The DVCon India ESL track reflects three key evolutionary changes:

Virtual platforms

- Modeling of designs in higher-level representations, most often with SystemC
- SystemC models in efficient virtual platforms to verify system behavior and performance
- Virtual platforms usually based on transaction-level modeling (TLM)

High-level synthesis

- Use of high-level synthesis (HLS) to generate RTL from SystemC models
- HLS models regarded as the golden source of the design
- HLS models sometimes refined from the virtual platform models

Hardware-software co-verification

- SoC teams verifying hardware and software portions of the design together
- Essential to verify system-level power management, safety, security, and performance
- IoT and self-driving vehicles demand a high level of full-system verification

Industry Trends Driving the DV Track

The DVCon India DV track reflects three key evolutionary changes:

UVM extensions

- Extensions to handle analog/mixed-signal (AMS) designs
- Extensions to support testbenches executing in hardware platforms
- Constrained-random stimulus and functional coverage for a wider range of designs

Formal techniques

- Static verification technologies in mainstream use
- Static tools range from “super-linters” to advanced formal analysis engines
- Formal proof important for system-level power management, safety, and security

Portable stimulus

- Software-driven verification with embedded processors rapidly gaining ground
- Portability from IP to SoC and from ESL to silicon next step beyond UVM
- Accellera working on a standard in this area

Highlights from DVCon 2015

In 2014, the first DVCon India was held in Bangalore, and it was surprisingly successful for a brand-new conference. More than 450 attendees from more than 80 companies and organizations attended the technical sessions, visited the exhibitors, and networked with each other. The event was bigger and better last year, growing to more than 600 attendees and an even broader technical program.

One highlight for 2015 was the set of keynote addresses from industry leaders. Speakers from LG Electronics, Continental, Infineon and others discussed the key challenges in the development of electronic products and the “Make in India” movement. Attendees then selected from a dozen tutorials and more than 50 papers and poster sessions to dig deeper into technical of interest. More than 20 vendors staffed their exhibition booths with experts who could discuss how their solutions could use the technologies covered in the technical sessions to address the challenges outlined in the keynotes. Finally, the program offered multiple opportunities for networking and social activity. Feedback was very positive; it is clear from these photos that attendees had a productive and enjoyable time:


MENTOR GRAPHICS

DVCon India 2016 is well positioned to be even more successful. The Technical Program Committee has spent countless hours reviewing submissions to build the best possible conference and many others have worked hard on logistics to ensure a smooth event. We look forward to seeing you in Bangalore in September!

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