

Start	End	General Sessions				Exhibit Areas
9:00	9:15	DVCon India 2022 Inauguration				
9:15	10:00	Vision Talk: Unleashing AI/ML for Faster Verification Closure <i>Manish Pandey, VP Engineering, Synopsys</i>				
10:00	10:30	Platinum Keynote: Emerging Design/Verification Technologies and Standards--Which comes first? <i>Dave Rich, Verification Architect, Siemens EDA</i>				
10:30	11:30	Panel: Verifying on the Bleeding Edge at Breakneck Speed <i>Intel</i>				
11:30	11:45	Tea Break & Networking				EXHIBIT HOURS 11:00am to 6:30pm
Start	End	Track 1	Track 2	Track 3	Track 4	
11:45	12:30	T1-A : Tutorial - Accelerate Time to ISO 26262 Compliance with Unified Functional Safety Verification <i>Synopsys</i>	T2-A : Short Workshop - Design space exploration of PIM (Process in Memory) /NMC (Near Memory compute) based on workload characterization. <i>Tata Consultancy Services</i>	T3-A : Short Workshop - SW.3A: Embracing Datapath Verification with Jasper C2RTL App <i>Cadence & NXP</i>	T4-A : Tutorial - Portable Stimulus Standard Update: PSS in the Real World <i>Accellera</i>	
12:30	13:15		T2-B : Short Workshop - Achieve Faster Debug Closure by Applying Big Data & Advanced RCA Technologies <i>Cadence & Western Digital</i>	T3-B : Short Workshop - SW.3B: Menta embedded FPGA (eFPGA): The Industry eFPGA soft IP fully customizable, for hardware reconfiguration in the field <i>Menta</i>		
13:15	14:15	Lunch Break				
14:15	14:45	Gold Keynote: <i>Cadence</i>				
14:45	15:15	Gold Keynote: Heterogeneous Integration in the AI Era <i>Subramani (Subi) Kengeri, Vice President, AI Systems Solutions, Applied Materials</i>				
15:15	15:30	Tea Break & Networking				
15:30	16:15	T1-C : Short Workshop - CXL 3.0 Overview <i>CXL Consortium</i>	T2-C : Short Workshop - SystemUVM™: Portable Stimulus Test Content Synthesis Advantages Without the Learning Curve <i>Breker Systems</i>	T3-C : Short Workshop - Intelligent Orchestration of EDA Resources <i>TCS</i>	T4-C : Tutorial - T.4B: Engaging with IEEE through Standards <i>IEEE</i>	
16:15	17:00	T1-D : Short Workshop -	T2-D : Short Workshop - GPU Modeling <i>Vayavya Labs</i>	T3-D : Short Workshop - IP/SoC Design, Co-Verify, Co-Validate, Co-Everything in 45 minutes! <i>Agnisys</i>		
17:00	18:30	Exhibits & Networking Reception				

Start	End	General Sessions				Poster Area
9:00	9:15	Welcome & TPC Update				
9:15	9:45	Platinum Keynote-2 <i>Tessolve</i>				
9:45	10:15	Platinum Keynote-3				
10:15	11:15	Panel: What will it take to fully implement a digital transformation platform for IP and services? <i>Siemens</i>				
11:15	11:30	Tea Break & Networking				Poster Hours 11:15am to 5:45pm
Start	End	Track 1	Track 2	Track 3	Track 4	
11:30	13:00	Paper Session 1A (FORMAL)	Paper Session 2A (Functional safety)	Paper Session 3A (ESL & Virtual type)	Paper Session 4A (New Design)	
11:30	12:00	1A1 - [3] Retry with Confidence: Use Formal Property Verification to Verify Link Layer Retry (LLR) Mechanism of Compute Express Link (CXL) <i>Anshul Jain, Aman Vyas, Sava Krstic, Binal Sodavadia and Achutha Kirankumar V M</i>	2A1 - [105] Fault Injection Strategy to Validate ASIL-D Requirements of BMS Components <i>Praneeth Uddagiri, Veera Satya Sai Gavimi and Prashantkumar Ravindra</i>	3A1 - [1] Novel Methodology for TLM Model Unit Verification <i>Navaneet Kumar, Archana Verma and Ashish Mathur</i>	4A1 - [65] Debug Time Reduction by Automatic Generation of Waiver List Using ML Techniques <i>Vardhana M, Akshay Jain and Kota Subba Rao Sajja</i>	
12:00	12:30	1A2 - [101] A Recipe for swift Tape-out of Derivative SoCs: A Comprehensive Validation Approach using Formal-based Sequential Equivalence and Connectivity Checking <i>Priyanshu Jain, Piyush Gupta, Sakef Gaddagi, Sandeep Kumar and Ipshita Tripathi</i>	2A2 - [97] What-If analysis of Safety Mechanism's impacts on ETHMAC design under Functional Safety flow <i>Udaykrishna J, Kapil Kumar, Gaurav Goel, Sujatha Hiremath and Sachin Pathak</i>	3A2 - [28] Methodology for system-level comparison of ARM vs RISC-V cores for latency and power consumption <i>Tom Jose and Deepak Shankar</i>	4A2 - [31] Disciplined post silicon validation using ML intelligence <i>Amaresh Chellapilla and Pandithurai Sangaiyah</i>	
12:30	13:00	1A3 - [25] The Formal way – Fast and Accurate Hashing Algorithm Verification <i>Sini Balakrishnan, Sireesha Tulluri, Bindumadhava Ss and Disha Puri</i>	2A3 - [108] A scalable framework to validate interconnect-based firewalls to enhance SoC security coverage <i>Ashutosh Mishra and Suresh Vasu</i>	3A3 - [61] Verification Reuse Strategy for RTL Quality SoC Functional Virtual Prototypes <i>Rajesh Jain, Gaurav Sharma, Marcel Achim, Ashish Mathur and Prateek Sikka</i>	4A3 - [76] Adaptive HW Trace Module for Complex SOCs for IoT Applications <i>Aarati Mehta</i>	
13:00	14:00	Lunch Break				
14:00	14:30	Gold Keynote: <i>Qualcomm</i>				
14:30	16:00	Paper Session 1B (FORMAL)	Paper Session 2B (Verification & Validation)	Paper Session 3B (Design reuse)	Paper Session 4B (RDC/CDC)	
14:30	15:00	1B1 - [11] OIL check of PCIe with Formal Verification <i>Vedprakash Mishra, Carlston Lim, Anshul Jain, Zhi Feng Lee, Jian Zhong Wang and Achutha Kirankumar V M</i>	2B1 - [32] Advancements in UVM Test Bench Architecture for Verifying High Speed MIPI PHY 5.0 IP <i>Eldhose P M, Sagar Jayakrishnan, Suraj Vijay Shetty, Kuntal Pandya and Parag S. Lonkar</i>	3B1 - [106] Novel Adaptive CPU Scoreboard Methodology for a Multi-language environment <i>Pooja Madhusoodhanan, Saya Goud Langadi and Labeeb K</i>	4B1 - [6] Bringing Reset Domains and Power Domains together – Non resettable registers amplifying issues in Power-Aware RDC Verification due to UPF Instrumentation <i>Manish Bhati and Inayat Ali</i>	
15:00	15:30	1B2 - [8] Effective Formal Deadlock Verification Methodologies for Interconnect design <i>Sachin Kumar and Rajesh C M</i>	2B2 - [19] Overcoming challenges in functional verification of Automotive traffic schedulers <i>Harshit Jaiswal, Hemlata Bist, Rohit Mishra and Ori Tal</i>	3B2 - [71] Scalable Test bench Architecture and Methodology for Faster Codec and Computer Vision Scenario Verification <i>Azhar Ahammad and Shreevara Murthy</i>	4B2 - [30] Innovative methodologies for analyzing CDC and RDC violations in complex SOCs using Automations, formal verification, and Hierarchical CDC model <i>Maitri Mishra and Dharmendra Kumar</i>	
15:30	16:00	1B3 - [54] Exhaustive validation of a cache memory controller using Formal Verification to meet performance and timing requirements <i>Himani Jawa, Nishant Raman, Manas Karanjekar and Sini Balakrishnan</i>	2B3 - [47] Shifting Left CXL Interop <i>John Shinto K S and Suhas Pai</i>	3B3 - [73] Efficient Regression Management with Smart Data Mining Technique <i>Tejbal Prasad</i>	4B3 - [87] Solving Problems with hierarchal CDC Analysis of digital SoC RTL with encrypted blocks <i>Abdul Moyeen, Arpita Agarwal, Aman Shaikh and Abhay Deshpande</i>	
16:00	16:15	Tea Break & Networking				
16:15	17:45	Paper Session 1C (FORMAL)	Paper Session 2C (Verification & Validation)	Paper Session 3C (Design reuse)	Paper Session 4C (Mixed signal)	
16:15	16:45	1C1 - [103] Novel approach for SoC pipeline latency and connectivity verification using formal <i>Deepak Mohan, Senthilnath Subbarayan and Sandeep Kumar</i>	2C1 - [23] UVM based Generic Interrupt Handler <i>Nikhil Singla and Debarati Banerjee</i>	3C1 - [9] An Efficient Methodology for Development of Cryptographic Engines <i>Sandesh Kanchodu, Tarun Rajendra Mittal, Sachin Kashyap and Subramanian Parameswaran</i>	4C1 - [52] Verifying the I/O peripherals of OpenTitan SOC using Portable Stimulus Standard <i>Mahesh R, Bidisha Das, Raj S Mitra, Loganath Ramachandran and Viraphol Chaiyakul</i>	
16:45	17:15	1C2 - [43] Enabling high quality design sign-off with Jasper structural and auto formal checks <i>Guruprasad Timmapur, Vishnu Haridas and Mansi Rastogi</i>	2C2 - [85] Configurable TB <i>Kilaru Vamsikrishna and Sushrut B Veerapur</i>	3C2 - [38] Accelerating the SoC Integration Verification Cycle Time Leveraging the Legacy Design Confidence <i>Abhinav Parashar and Prasanth Kumar Narava</i>	4C2 - [59] Logic Equivalence Check without Low Power – you are at risk <i>Aishwarya Nair and Krishna Patel</i>	
17:15	17:45	1C3 - [100] Efficient Formal strategies to verify the robustness of the design <i>Sakthivel Ramaiah</i>	2C3 - [7] Efficacious verification of Loopback and Equalization in PCIe By Using Novel approach <i>Jaydeep Suvariya and Pinal Patel</i>	3C3 - [99] A Generic Configurable Error Injection Agent for On-Chip Memories <i>Niharika Sachdeva, Arjun Suresh Kumar, Anil Deshpande, Somasunder Kattapura Sreenath and Raviteja Gopagiri</i>	4C3 - [93] Harnessing SV-RNM Based Modelling and Simulation Methodology for Verifying a Complex PMIC designed for SSD Applications <i>Vijay Kumar, Shrikant Pattar, Yaswanth Chebrolu and Vinayak Hegde</i>	
17:45	18:15	Awards & Closing				