### Monday, September 5, 2022

**General Sessions - Grand Victoria**

**DVCon India 2022 Inauguration**

**Vision Talk: Unleashing AI/ML for Faster Verification Closure**
- Manish Pandey, VP Engineering, Synopsys

**Keynote: Emerging Design/Verification Technologies and Standards--Which comes first?**
- Dave Rich, Verification Architect, Siemens EDA

**Panel: Verifying on the Bleeding Edge at Breakneck Speed**
- Sukumar Raghuram, Rivos, Inc; Dennis Brrophy, Siemens EDA; Suraj Kamat, ARM; Pradeep Babu, Qualcomm; Yuadhishthira Kundra, Intel [Moderator]

**Tea Break & Networking**

<table>
<thead>
<tr>
<th>Start</th>
<th>End</th>
<th>Track 1 - Grand Victoria B</th>
<th>Track 2 - Grand Victoria A</th>
<th>Track 3 - Robusta</th>
<th>Track 4 - Arabica</th>
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</thead>
<tbody>
<tr>
<td>12:30</td>
<td>13:15</td>
<td></td>
<td>T2-B: Short Workshop - Achieve Faster Debug Closure by Applying Big Data &amp; Advanced RCA Technologies Cadence &amp; Western Digital</td>
<td>T3-B: Short Workshop - SW.3B: Menta embedded FPGA (eFPGA): The Industry eFPGA soft IP fully customizable, for hardware reconfiguration in the field Menta</td>
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**Lunch Break**

- **Keynote: Verification: A Critical Enabler for the $Trillion Chip Design Industry**
  - Lokesh Babu, AE Director, Cadence

- **Keynote: Heterogeneous Integration in the AI Era**
  - Subramani (Subi) Kengeri, Vice President - AI Systems Solutions, Applied Materials

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<tr>
<td>15:30</td>
<td>16:15</td>
<td>T1-C: Short Workshop - CXL 3.0 Overview CXL Consortium</td>
<td>T2-C: Short Workshop - SystemUVM™: Portable Stimulus Test Content Synthesis Advantages Without the Learning Curve Breker Systems</td>
<td>T3-C: Short Workshop - Intelligent Orchestration of EDA Resources TCS</td>
<td>T4-C: Tutorial - Engaging with IEEE through Standards IEEE</td>
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<tr>
<td>16:15</td>
<td>17:00</td>
<td>T1-D: Short Workshop - Hardware Security – Industry Trends, Attacks and Solutions Microchip</td>
<td>T2-D: Short Workshop - GPU Modeling Vayavya Labs</td>
<td>T3-D: Short Workshop - IP/SoC Design, Co-Verify, Co-Validate, Co-Everything in 45 minutes! Agnisys</td>
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| 17:00 | 18:30| | | | | **Exhibits & Networking Reception**

**EXHIBIT HOURS**

11:00am to 6:30pm
### Tuesday, September 6, 2022

#### General Sessions - Grand Victoria

<table>
<thead>
<tr>
<th>Time</th>
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<tbody>
<tr>
<td>9:00</td>
<td>Welcome &amp; IPC Update</td>
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<tr>
<td>9:15</td>
<td>Keynote: Verification Challenges, Trends and Their Practical Adoption – ASIC Manager’s Perspective</td>
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<tr>
<td>9:45</td>
<td>Break</td>
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<tr>
<td>10:15</td>
<td>Keynote: Verification Challenges in Rapidly Evolving Ecosystem</td>
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<tr>
<td>10:45</td>
<td>Joy Chandra, Senior Director of Engineering, Qualcomm</td>
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<tr>
<td>11:15</td>
<td>Panel: What will it take to fully implement a digital transformation platform for tools, IP, and services? Sanjeev Kumar, Logic Fruit; SriVamsa Daruvanshi, Motive; Vijay Patil, Kannan, Vector; Shreemahin Acharya, Excellent &amp; Shreekul Jeeawoody, Siemens EDA (Moderator)</td>
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#### Track 1 - Grand Victoria B

<table>
<thead>
<tr>
<th>Time</th>
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<tbody>
<tr>
<td>11:30</td>
<td>Paper Session 1A (Formal)</td>
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<tr>
<td>12:00</td>
<td>Paper Session 1B (Formal)</td>
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<tr>
<td>12:30</td>
<td>Paper Session 1C (Formal)</td>
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<tr>
<td>13:00</td>
<td>Paper Session 1D (Formal)</td>
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#### Track 2 - Grand Victoria A

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<tr>
<th>Time</th>
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<tbody>
<tr>
<td>11:30</td>
<td>Paper Session 2A (Formal)</td>
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<tr>
<td>12:00</td>
<td>Paper Session 2B (Formal)</td>
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<tr>
<td>12:30</td>
<td>Paper Session 2C (Formal)</td>
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<td>Paper Session 2D (Formal)</td>
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<tbody>
<tr>
<td>11:30</td>
<td>Paper Session 3A (ESL &amp; Virtual type)</td>
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<tr>
<td>12:00</td>
<td>Paper Session 3B (ESL &amp; Virtual type)</td>
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<tr>
<td>12:30</td>
<td>Paper Session 3C (ESL &amp; Virtual type)</td>
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<tr>
<td>13:00</td>
<td>Paper Session 3D (ESL &amp; Virtual type)</td>
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#### Track 4 - Arabiaica

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<tr>
<td>11:30</td>
<td>Paper Session 4A (New Design)</td>
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<tr>
<td>12:00</td>
<td>Paper Session 4B (CDC/RDC)</td>
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<tr>
<td>12:30</td>
<td>Paper Session 4C (Mixed Signal)</td>
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<tr>
<td>13:00</td>
<td>Paper Session 4D (Mixed Signal)</td>
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#### Lunch Break

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#### Posters and Exhibitor Visit

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#### Awards & Closing

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**Track 1 - Grand Victoria B**

**Paper Session 1A (Formal)**

1. "[9] Retrying with Confidence: UML Formal Property Verification to Verify Link Layer Retry (LLR) Mechanism of Compute Express Link (CXL)

2. "[10] Fault Injection Strategy to Validate ASIL-D Requirements of BMS Components"

3. "[11] Novel Methodology for TLM Model Unit Verification"

4. "[12] Debug Time Reduction by Automatic Generation of Waiver Statements"

**Paper Session 1B (Formal)**


2. "[14] Scalable Framework to Validate Interconnect-based Firewalls to Enhance SoC Security Coverage"


4. "[16] Efficient Regression Management with Smart Indexing"

**Paper Session 1C (Formal)**

1. "[17] Novel Approach for SoC Power Optimization: Cycle Time Leveraging the Legacy Design Confidence"

2. "[18] Efficient Formal Deadlock Verification Methodologies for Interconnect Design"

3. "[19] Novel Adaptation of CPU Scoreboard Methodologies for DDR5 Memory Design Environment"

4. "[20] Innovative Methodologies for Analyzing CDC and RVC Violations in Complex SOCs Using Automations, Formal Verification, and Hierarchical CDC Model"

**Paper Session 1D (Formal)**

1. "[21] Hierarchical CDC model for Verifying High Speed MIPI MPHY 5.0 IP"

2. "[22] Scenario Verification: Superpower Using ML Techniques"


4. "[24] Evaluating Safety Mechanism’s Impacts on Driver Design for Power Management System"