Monday, September 5, 2022

DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION INDIA

Start	End	General Sessions - Grand Victoria	Exhibit Areas
9:00	9:15	**DVCon India 2022 Inauguration**	
9:15	10:00	**Vision Talk: Unleashing AI/ML for Faster Verification Closure** *Manish Pandey, VP Engineering, Synopsys*	
10:00	10:30	**Keynote: Emerging Design/Verification Technologies and Standards--Which comes first?** *Dave Rich, Verification Architect, Siemens EDA*	
10:30	11:30	**Panel: Verifying on the Bleeding Edge at Breakneck Speed** *Sukumar Raghuram, Rivos, Inc; Dennis Brophy, Siemens EDA; Suraj Kamat, ARM; Pradeep Babu, Qualcomm; Yudhishthira Kundu, Intel (Moderator)*	
11:30	11:45	**Tea Break & Networking**	EXHIBIT HOURS 11:00am to 6:30pm

Start	End	Track 1 - Grand Victoria B	Track 2 - Grand Victoria A	Track 3 - Robusta	Track 4 - Arabica
11:45	12:30	T1-A : Tutorial - **Accelerate Time to ISO 26262 Compliance with Unified Functional Safety Verification** *Synopsys*	T2-A : Short Workshop - **Design space exploration of PIM (Process in Memory) /NMC (Near Memory compute) based on workload characterization.** *Tata Consultancy Services*	T3-A : Short Workshop - SW.3A: **Embracing Datapath Verification with Jasper C2RTL App** *Cadence & NXP*	T4-A : Tutorial - **Portable Stimulus Standard Update: PSS in the Real World** *Accellera*
12:30	13:15		T2-B : Short Workshop - **Achieve Faster Debug Closure by Applying Big Data & Advanced RCA Technologies** *Cadence & Western Digital*	T3-B : Short Workshop - SW.3B: **Menta embedded FPGA (eFPGA): The Industry eFPGA soft IP fully customizable, for hardware reconfiguration in the field** *Menta*	
13:15	14:15	**Lunch Break**			
14:15	14:45	**Keynote: Verification: A Critical Enabler for the $Trillion Chip Design Industry** *Lokesh Babu, AE Director, Cadence*			
14:45	15:15	**Keynote: Heterogeneous Integration in the AI Era** *Subramani (Subi) Kengeri, Vice President - AI Systems Solutions, Applied Materials*			
15:15	15:30	**Tea Break & Networking**			
15:30	16:15	T1-C : Short Workshop - **CXL 3.0 Overview** *CXL Consortium*	T2-C : Short Workshop - **SystemUVM™: Portable Stimulus Test Content Synthesis Advantages Without the Learning Curve** *Breker Systems*	T3-C : Short Workshop - **Intelligent Orchestration of EDA Resources** *TCS*	T4-C : Tutorial - **Engaging with IEEE through Standards** *IEEE*
16:15	17:00	T1-D : Short Workshop - **Hardware Security – Industry Trends, Attacks and Solutions** *Microchip*	T2-D : Short Workshop - **GPU Modeling** *Vayavya Labs*	T3-D : Short Workshop - **IP/SoC Design, Co-Verify, Co-Validate, Co-Everything in 45 minutes!** *Agnisys*	
17:00	18:30	**Exhibits & Networking Reception**			

Tuesday, September 6, 2022

DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION INDIA

Start	End	General Sessions - Grand Victoria	Poster Area
9:00	9:15	**Welcome & TPC Update**	
9:15	9:45	**Keynote: Verification Challenges, Trends and their Practical Adoption – An ASIC Manager's Perspective** *Madhav Rao, SVP - VLSI BU, Tessolve Semiconductor Pvt. Ltd.*	
9:45	10:15	**Keynote: Verification Challenges in Rapidly Evolving Ecosystem** *Joy Chandra, Senior Director of Engineering, Qualcomm*	
10:15	11:15	**Panel: What will it take to fully implement a digital transformation platform for tools, IP and services?** *Sanjeev Kumar, Logic Fruit; Srinivasan Duraiswamy, Mobiveil; Shripad Kanni, Vector; Shrinath Acharya, Excelfore & Shakeel Jeeawoody, Siemens EDA (Moderator)*	
11:15	11:30	**Tea Break & Networking**	

Start	End	Track 1 - Grand Victoria B	Track 2 - Grand Victoria A	Track 3 - Robusta	Track 4 - Arabica	Poster Area
11:30	13:00	**Paper Session 1A (Formal)**	**Paper Session 2A (Functional safety)**	**Paper Session 3A (ESL & Virtual type)**	**Paper Session 4A (New Design)**	**Poster Hours 11:15am to 5:45pm**
11:30	12:00	**1A1** - [3] Retry with Confidence: Use Formal Property Verification to Verify Link Layer Retry (LLR) Mechanism of Compute Express Link (CXL) *Anshul Jain, Aman Vyas, Sava Krstic, Binal Sodavadia and Achutha Kirankumar V M*	**2A1** - [105] Fault Injection Strategy to Validate ASIL-D Requirements of BMS Components *Praneeth Uddagiri, Veera Satya Sai Gavirni and Prashantkumar Ravindra*	**3A1** - [1] Novel Methodology for TLM Model Unit Verification *Navaneet Kumar, Archna Verma and Ashish Mathur*	**4A1** - [65] Debug Time Reduction by Automatic Generation of Waiver List Using ML Techniques *Vardhana M, Akshay Jain and Kota Subba Rao Sajja*	
12:00	12:30	**1A2** - [101] A Recipe for swift Tape-out of Derivative SoCs: A Comprehensive Validation Approach using Formal-based Sequential Equivalence and Connectivity Checking *Priyanshu Jain, Piyush Gupta, Saket Gaddagi, Sandeep Kumar and Ipshita Tripathi*	**2A2** - [97] What-If analysis of Safety Mechanism's impacts on ETHMAC design under Functional Safety flow *Udaykrishna J, Kapil Kumar, Gaurav Goel, Sujatha Hiremath and Sachin Pathak*	**3A2** - [28] Methodology for system-level comparison of ARM vs RISC-V cores for latency and power consumption *Tom Jose and Deepak Shankar*	**4A2** - [31] Disciplined post silicon validation using ML intelligence *Amaresh Chellapilla and Pandithurai Sangaiyah*	
12:30	13:00	**1A3** - [25] The Formal way – Fast and Accurate Hashing Algorithm Verification *Sini Balakrishnan, Sireesha Tulluri, Bindumadhava Ss and Disha Puri*	**2A3** -[108] A scalable framework to validate inteconnect-based firewalls to enhance SoC security coverage *Ashutosh Mishra and Suresh Vasu*	**3A3** - [61] Verification Reuse Strategy for RTL Quality SoC Functional Virtual Prototypes *Rajesh Jain, Gaurav Sharma, Marcel Achim, Ashish Mathur and Prateek Sikka*	**4A3** - [57] Left shift catching of critical low power bugs with Formal Verification *Manish Kumar, Madan Kumar, Srobona Mitra, Madhusudhana Lebaka*	
13:00	14:00	**Lunch Break**				
14:00	14:30	**Posters and Exhibitor Visit**				
14:30	16:00	**Paper Session 1B (Formal)**	**Paper Session 2B (Verification & Validation)**	**Paper Session 3B (Design Resue)**	**Paper Session 4B (CDC/RDC)**	
14:30	15:00	**1B1** - [11] OIL check of PCIe with Formal Verification *Vedprakash Mishra, Carlston Lim, Anshul Jain, Zhi Feng Lee, Jian Zhong Wang and Achutha Kirankumar V M*	**2B1** - [32] Advancements in UVM Test Bench Architecture for Verifying High Speed MIPI MPHY 5.0 IP *Eldhose P M, Sagar Jayakrishnan, Suraj Vijay Shetty, Kuntal Pandya and Parag S. Lonkar*	**3B1** - [106] Novel Adaptive CPU Scoreboard Methodology for a Multi-language environment *Pooja Madhusoodhanan, Saya Goud Langadi and Labeeb K*	**4B1** - [6] Bringing Reset Domains and Power Domains together – Non resettable registers amplifying issues in Power-Aware RDC Verification due to UPF Instrumentation *Manish Bhati and Inayat Ali*	
15:00	15:30	**1B2** - [8] Effective Formal Deadlock Verification Methodologies for Interconnect design *Sachin Kumar and Rajesh C M*	**2B2** - [19] Overcoming challenges in functional verification of Automotive traffic schedulers *Harshit Jaiswal, Hemlata Bist, Rohit Mishra and Ori Tal*	**3B2** - [71] Scalable Test bench Architecture and Methodology for Faster Codec and Computer Vision Scenario Verification *Azhar Ahammad and Shreekara Murthy*	**4B2** - [30] Innovative methodologies for analyzing CDC and RDC violations in complex SOCs using Automations, formal verification, and Hierarchical CDC model *Maitri Mishra and Dharmendra Kumar*	
15:30	16:00	**1B3** - [54] Exhaustive validation of a cache memory controller using Formal Verification to meet performance and timing requirements *Himani Jawa, Nishant Raman, Manas Karanjekar and Sini Balakrishnan*	**2B3** - [47] Shifting Left CXL Interop *John Shinto K S and Suhas Pai*	**3B3** - [73] Efficient Regression Management with Smart Data Mining Technique *Tejbal Prasad*	**4B3** - [87] Solving Problems with hierarchal CDC Analysis of digital SoC RTL with encrypted blocks *Abdul Moyeen, Arpita Agarwal, Aman Shaikh and Abhay Deshpande*	
16:00	16:15	**Tea Break & Networking**				
16:15	17:45	**Paper Session 1C (Formal)**	**Paper Session 2C (Verification & Validation)**	**Paper Session 3C (Design Reuse)**	**Paper Session 4C (Mixed Signal)**	
16:15	16:45	**1C1** - [103] Novel approach for SoC pipeline latency and connectivity verification using formal *Deepak Mohan, Senthilnath Subbarayan and Sandeep Kumar*	**2C1** - [23] UVM based Generic Interrupt Handler *Nikhil Singla and Debarati Banerjee*	**3C1** - [9] An Efficient Methodology for Development of Cryptographic Engines *Sandesh Kanchodu, Tarun Rajendra Mittal, Sachin Kashyap and Subramanian Parameswaran*	**4C1** - [52] Verifying the I/O peripherals of OpenTitan SOC using Portable Stimulus Standard *Mahesh R, Bidisha Das, Raj S Mitra, Loganath Ramachandran and Viraphol Chaiyakul*	
16:45	17:15	**1C2** - [43] Enabling high quality design sign-off with Jasper structural and auto formal checks *Guruprasad Timmapur, Vishnu Haridas and Mansi Rastogi*	**2C2** - [85] Configurable TB *Kilaru Vamsikrishna and Sushrut B Veerapur*	**3C2** - [38] Accelerating the SoC Integration Verification Cycle Time Leveraging the Legacy Design Confidence *Abhinav Parashar and Prasanth Kumar Narava*	**4C2** - [59] Logic Equivalence Check without Low Power – you are at risk *Aishwarya Nair and Krishna Patel*	
17:15	17:45	**1C3** - [100] Efficient Formal strategies to verify the robustness of the design *Sakthivel Ramaiah*	**2C3** - [7] Efficacious verification of Loopback and Equalization in PCIe By Using Novel approach *Jaydeep Suvariya and Pinal Patel*	**3C3** - [99] A Generic Configurable Error Injection Agent for On-Chip Memories *Niharika Sachdeva, Arjun Suresh Kumar, Anil Deshpande, Somasunder Kattepura Sreenath and Raviteja Gopagiri*	**4C3** - [93] Harnessing SV-RNM Based Modelling and Simulation Methodology for Verifying a Complex PMIC designed for SSD Applications *Vijay Kumar, Shrikant Pattar, Yaswanth Chebrolu and Vinayak Hegde*	
17:45	18:15	**Awards & Closing**				