Wednesday, September 13, 2023

DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION INDIA

Start	End	General Sessions - Grand Victoria	Exhibit Areas
9:00	9:15	**DVCon India 2023 Inauguration**	
9:15	10:00	**Vision Talk: Autonomous Verification: Are we there yet?** *Sandeep Mehrotra, VP Engineering, Synopsys*	
10:00	10:30	**Keynote: Smart Verification: Faster is not enough!** *Abhi Kolpekwar, VP & GM – DVT, Siemens EDA*	
10:30	11:30	**Industry Panel: Closing DV Gaps in ever increasing SOC Design size Vs shrinking Time to Market** *Cadence*	
11:30	11:45	**Tea Break & Networking**	**EXHIBIT HOURS 11:00am to 6:30pm**

Start	End	Track 1 - Grand Victoria B	Track 2 - Grand Victoria A	Track 3 – Robusta & Arabica	Track 4 - Brainbox
11:45	12:30	Tutorial 1A: **Static Signoff Best Practices – Learnings and experiences from industry use cases** *Real Intent*	Tutorial 2A: **Improving Debug Productivity using latest AI & ML Techniques** *Cadence*	Short Workshop 3A_1: *Accellera*	Short Workshop 4A_1: **Identifying and overcoming Multi-Die System Verification Challenges** *Synopsys*
12:30	13:15			Short Workshop 3A_2: **Advanced Core/SoC Verification for RISC-V and Other Cores** *Breker*	Short Workshop 4A_2: **Accelerating heterogeneous SoC designs with prebuilt blueprints and cloud hardware assisted emulation and prototyping** *SoC.one*
13:15	14:15	**Lunch Break**			
14:15	14:45	**Keynote: Journeying Beyond AI: Unleashing the Art of Verification** *P R Sivakumar, Founder and CEO, Maven Silicon*			
14:45	15:15	**Keynote: AI for Chip Design: Scaling DV Capacity to Meet Massive Demand Growth** *Dr. Ziyad Hanna, GM-Israel, Cadence*			
15:15	15:45	**Keynote: Bugs, Transistors, Chips, and Waves - A Panoramic View of the Journey from Four to a Quintillion, and Beyond** *Vishwanath Ananthakrishnan, SVP & GM, Mirafra*			
15:45	16:00	**Tea Break & Networking**			
16:00	16:45	Tutorial 1B: **Taking the first steps towards verifying billion gate designs with formal methods** *Axiomise*	Tutorial 2B: **Fast track RISC-V System Validation Using Hardware Assisted Verification Platforms** *Synopsys*	Short Workshop 3B_1: **Automation of Realisation Layer for IP/SoC using PSS & SystemRDL** *Agnisys*	Short Workshop 4B_1: **An Overview of Ethernet 10Base-T1S in Automotive SoCs and its Verification** *Synopsys & ST Microelectronics*
16:45	17:30			Short Workshop 3B_2: **CXL Verification using Portable Stimulus** *Vayavya*	Short Workshop 4B_2: **UCIe based Design Verification** *Cadence*
17:30	19:00	**Exhibits & Networking Reception**			

Thursday, September 14, 2023

DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION INDIA

Start	End	General Sessions - Grand Victoria	Poster Area
9:00	9:15	**Welcome & TPC Update**	
9:15	9:45	**Keynote:** *Tessolve Semiconductor Pvt. Ltd.*	
9:45	10:15	**Keynote:** *Qualcomm*	
10:15	11:15	**Industry Panel: Revolutionizing System-Level Verification and Validation: Implications for India's Innovation Drive** *Siemens EDA*	
11:15	11:30	**Tea Break & Networking**	

Start	End	Track 1 - Grand Victoria B	Track 2 - Grand Victoria A	Track 3 – Robusta & Arabica	Track 4 - Brainbox
11:30	13:00	**Paper Session 1A (New Design Ideas & Disruptive Trends)**	**Paper Session 2A (Formal Verification)**	**Paper Session 3A (Design & Verif. Reuse & Automation)**	**Paper Session 4A (Mixed Signal & Low Power)**
11:30	12:00	**1A1** - **[8717]** No gain without RISC- A novel approach for accelerating and streamlining RISC-V Processor functional verification with register change dump methodology.	**2A1** – **[628]** Revolutionizing Proof Convergence for Algorithmic Designs: Combining Multiple Formal Verification Tools	**3A1** – **[9578]** Coverage Acceleration and Testcase Pruning using Smart Stimuli Generator in SOC Verification	**4A1** - **[3422]** Wrong clamps can kill your chip!!.... find them early
12:00	12:30	**1A2** - **[5538]** Code-Test-Verify all for free – Assertions + Verilators	**2A2** - **[9536]** Quiescent Formal Checks (QFC) for Detecting Deep Design Bugs – Sooner and Faster	**3A2** – **[6347]** Efficient Verification of Arbitration Design with a Generic Model	**4A2** – **[9423]** Robust Low Power Verification Strategy for a Complex 3DIC System with Split Power Management Architecture
12:30	13:00	**1A3** - **[1971]** Efficacious Verification of Irreproachable and Steady Data Transfer Protocol for high-speed die-to-die communication on a 3DIC Chip	**2A3** – **[6042]** FV: A Robust Solution for Tackling Design Complexities –A Case Study on In-Band ECC	**3A3** – **[6533]** - Python empowered GLS Bringup Vehicle	**4A3** – **[5290]** Fast Convergence Modular Advanced Smart-Hybrid Testbench (FCMAST) to automate and expedite SoC gate level simulations closure
13:00	14:00	**Lunch Break**			
14:00	14:30	**Posters and Exhibitor Visit**			
14:30	16:00	**Paper Session 1B (Verification & Validation)**	**Paper Session 2B (Formal Verification)**	**Paper Session 3B (Design & Verif. Reuse & Automation)**	**Paper Session 4B (Functional Safety & Security)**
14:30	15:00	**1B1** – **[6285]** Netlist Enabled Emulation Platform for Accelerated Gate Level Verification	**2B1** – **[779]** Pseudo–LRU Not Efficient in Real World? Use Formal Verification to Bridge the Gap	**3B1** – **[8516]** Tackling the verification complexities of a processor subsystem through Portable stimulus	**4B1** – **[9164]** Holistic Verification of Bus Health Monitor in Automotive SoC using BHMVC and ParaHunter
15:00	15:30	**1B2** – **[2304]** A Faster and Efficient Constraint Verification Methodology for GFX SOCs	**2B2** – **[264]** Paradigm Shift In Power Aware Simulation Using Formal Techniques	**3B2** - **[285]** UVM Sequence Layering for Register Sequences	**4B2** – **[2784]** RISC V Subsystem Diagnostic Coverage Closure Flow for ASIL D
15:30	16:00	**1B3** - **[2910]** Breaking Down Barriers: Achieving Seamless Protocol Conversion with UVM Component Layering	**2B3** – **[2523]** Covering all the bases: Coverage-driven Formal Verification Sign-off of Pipelined Error Detection Filter	**3B3** – **[1126]** HISIG- An Efficient Gate Level Simulation Flow for a Hard IP Inside a Soft IP	**4B3** – **[9612]** Formal Verification + CIA Triad: Winning Formula for Hardware Security
16:00	16:15	**Tea Break & Networking**			
16:15	17:45	**Paper Session 1C (Verification & Validation)**	**Paper Session 2C (Formal Verification)**	**Paper Session 3C (Design & Verif. Reuse & Automation)**	**Paper Session 4C (Static Verification)**
16:15	16:45	**1C1** – **[4003]** Tabled Data Into Query Able Data key concepts demonstrated using DDR5 example	**2C1** – **[2546]** When Last Minute Formal Verification Strikes Gold: A Case Study on Finding Starvations and Deadlocks in a Project nearing Tape-in using RTL embedded assertions	**3C1** – **[2750]** Performance Analysis and Acceleration of High Bandwidth Memory System	**4C1** – **[1147]** Statistical Analysis of Clock Domain Crossings
16:45	17:15	**1C2** – **[6862]** A Generic Verification Methodology for Chip to Chip Interrupt Handling in a Multi-Chip SoC (3DIC)	**2C2** – **[6610]** Raising the Bar: Achieving Formal Verification Sign-Off for Complex Algorithmic Designs, with a Dot Product Accumulate Case Study	**3C2** – **[3142]** An Efficient Verification Methodology to Achieve DV Sign-off with Emphasis on Quality and Quicker DV Cycle	**4C2** – **[3353]** PropGen: An Automated Flow to Generate SVA Properties for Formal and Simulation methods
17:15	17:45	**1C3 - [8579]** Automotive RADAR bitfields Verification to support Validation of Silicon bring-up	**2C3** – **[4818]** Accelerating SoC Sensor Network Verification Sign-off through Dynamic Simulation and Formal Verification Synergy	**3C3** – **[6744]** Disaggregated methodology in Multi-die SoC– A Server SoC Case Study	**4C3** – **[2722]** Techniques to identify reset metastability issues due to soft resets
17:45	18:15	**Awards & Closing**			

Poster Hours 11:15am to 5:45pm