Wednesday, September 13, 2023

DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION INDIA

Start	End	General Sessions - Grand Victoria	Exhibit Areas
9:00	9:15	**DVCon India 2023 Inauguration**	
9:15	10:00	**Vision Talk: Autonomous Verification: Are we there yet?** *Sandeep Mehrotra, VP Engineering, Synopsys*	
10:00	10:30	**Keynote: Smart Verification: Faster is not enough!** *Abhi Kolpekwar, VP & GM – DVT, Siemens EDA*	
10:30	11:30	**Industry Panel: Closing DV Gaps in ever increasing SOC Design size Vs shrinking Time to Market** *Panelists: Siva Kumar, Microsoft; Garima Srivastava, Samsung; Sundar PH, Western Digital; Sushrut Veerapur, Cadence; Moderator: Anika Sunda, Cadence*	
11:30	11:45	**Tea Break & Networking**	

Start	End	Track 1 - Grand Victoria B	Track 2 - Grand Victoria A	Track 3 – Robusta & Arabica	Track 4 - Marquis	
11:45	12:30	Tutorial 1A: **Static Signoff Best Practices – Learnings and experiences from industry use cases** *Real Intent*	Tutorial 2A: **Improving Debug Productivity using latest AI & ML Techniques** *Cadence*	Short Workshop 3A_1: **Accellera's Latest Updates and a Look Forward** *Accellera*	Short Workshop 4A_1: **Identifying and overcoming Multi-Die System Verification Challenges** *Synopsys*	
12:30	13:15			Short Workshop 3A_2: **Advanced Core/SoC Verification for RISC-V and Other Cores** *Breker*	Short Workshop 4A_2: **Accelerating heterogeneous SoC designs with prebuilt blueprints and cloud hardware assisted emulation and prototyping** *SoC.one*	
13:15	14:15	**Lunch Break**				
14:15	14:45	**Keynote: Journeying Beyond AI: Unleashing the Art of Verification** *P R Sivakumar, Founder and CEO, Maven Silicon*				
14:45	15:15	**Keynote: AI for Chip Design: Scaling DV Capacity to Meet Massive Demand Growth** *Dr. Ziyad Hanna, GM-Israel, Cadence*				
15:15	15:45	**Keynote: Bugs, Transistors, Chips, and Waves - A Panoramic View of the Journey from Four to a Quintillion, and Beyond** *Vishwanath Ananthakrishnan, SVP & GM, Mirafra*				
15:45	16:00	**Tea Break & Networking**				
16:00	16:45	Tutorial 1B: **Taking the first steps towards verifying billion gate designs with formal methods** *Axiomise*	Tutorial 2B: **Fast track RISC-V System Validation Using Hardware Assisted Verification Platforms** *Synopsys*	Short Workshop 3B_1: **Automation of Realisation Layer for IP/SoC using PSS & SystemRDL** *Agnisys*	Short Workshop 4B_1: **An Overview of Ethernet 10Base-T1S in Automotive SoCs and its Verification** *Synopsys & ST Microelectronics*	
16:45	17:30			Short Workshop 3B_2: **CXL Verification using Portable Stimulus** *Vayavya*	Short Workshop 4B_2: **UCIe based Design Verification** *Cadence*	
17:30	17:45	**Day 1 Closing Remarks**				
17:45	19:00	**Drinks & Networking**				
19:00	19:10	**DVCon India 2023 Awards Welcome**				
19:10	20:00	**Leadership Talk: Force Multiplier** Major Deepak Iyer, Founder and CEO, Mastery Inside				
20:00	20:15	**DVCon India 2023 Awards**				
20:15	22:00	**Dinner**				

EXHIBIT HOURS

11:00am to 10:00pm