

Wednesday, September 18, 2024

Start	End	General Sessions - Grand Victoria				Exhibit Areas
09:00	09:15	DVCon India 2024 Inauguration				
09:15	10:00	Vision Talk: <i>Empowering Innovation: Harnessing Collective Wisdom across Tools, Processes, and People!</i> Harry Foster, Siemens				
10:00	10:30	Keynote: <i>The Increasing Verification Horizon in the Era of Pervasive Intelligence</i> Vikas Gautam, Synopsys & Subrangshu Das, Google				
10:30	11:15	Industry Panel: <i>Strengthening India's Fab Ecosystem: The Critical Role of the Design Community</i>				
11:15	11:30	Tea Break & Networking				
Start	End	Track 1 - Grand Victoria B	Track 2 - Grand Victoria A	Track 3 - Robusta & Arabica	Track 4 - Brain Box	EXHIBIT HOURS 11:00am to 6:30pm
11:30	12:15	Tutorial 1A: Expanding role of Static Signoff in Verification Coverage <i>Vikas Sachdeva, Real Intent</i>	Tutorial 1A: Next Generation Debug <i>Rohit Ohlayan and Prasad Chelur, Synopsys</i>	Short Workshop 3A_1: Find and Fix Excessive Power Dissipation of your Chip Very Early in the Design Cycle <i>Mohammed Fahad, Siemens</i>	Short Workshop 4A_1: What's new in SystemC 3.0 - IEEE 1666-2023 <i>Umesh Sisodia, CircuitSutra</i>	
12:15	13:00			Short Workshop 3A_2: Power Dynamics: Shaping the Future of the Data-Centric Era <i>Vijay Chobisa and Gaurav Saharawat, Siemens</i>	Short Workshop 4A_2: Harnessing AI for Enhanced Verification Efficiency <i>Anika Sunda, Cadence</i>	
13:00	14:00	Lunch Break				
14:00	14:30	Keynote: <i>AI for Verification – Today's Reality Vs. Tomorrow's Promisedence</i> Matt Graham, Cadence				
14:30	15:00	Keynote: <i>The Future is Formal</i> Ashish Darbari, Axiomise				
15:15	15:45	Keynote: <i>Navigating the Future of Chip Design Verification in an Era of Rapid Semiconductor Innovation</i> Apurva Kumar, Quest Global				
15:45	16:00	Tea Break & Networking				
16:00	16:45	Tutorial 1B: Update by Accellera CDC Standardization	Short Workshop 2B_1: High performance design verification techniques <i>Arun Joseph and Puja Sethia, IBM</i>	Short Workshop 3B_1: Functional Safety and High reliability in FPGA design <i>Nilesh Shilankar and Manohar Reddy Vadicherla, Synopsys</i>	Short Workshop 4B_1: RISC- V adoption in India <i>Priyanka Das, Aarfive</i>	
16:45	17:30		Short Workshop 2B_2: Portable Stimulus and VIP: Like a Hand in a Glove <i>Pradeep Salla, Raghavendra HM, Siemens</i>	Short Workshop 3B_2: FPGA Prototyping for Large Multi-Die/Multi-Core Designs <i>Madhav Chikodikar and Subhankar Ghosh, Synopsys</i>	Short Workshop 4B_2: RISC-V Ecosystem <i>Libin, CDAC</i>	
17:30	17:45	Day 1 Closing Remarks				
17:45	19:00	Drinks & Networking				
19:00	19:10	DVCon India 2024 Awards Welcome - Tessolve				
19:10	20:00	Leadership Talk: <i>Awake Thyself</i> Arjun Devaiah, International Athlete & National Sprint Champion				
20:00	20:30	DVCon India 2024 Awards				
20:30	22:00	Dinner				