

Start	End	General Sessions - Grand Victoria				
09:00	09:15	Welcome & TPC Update				
09:15	09:45	Keynote: Accelerated Infrastructure in an AI World Puneet Agarwal, Marvell				
09:45	10:15	Keynote: Qualcomm				
10:15	11:00	Industry Panel: Building RISC-V Systems: An Indian Perspective				
11:00	11:15	Tea Break & Networking				
Start	End	Track 1 - Grand Victoria B	Track 2 - Grand Victoria A	Track 3 - Robusta & Arabica	Track 4 - Brain Box	Track 5 - Marquis
11:15	12:45	Paper Session 1A: Design & Architecture	Paper Session 2A: Formal Verification	Paper Session 3A: Design Verification - SV & UVM	Paper Session 4A: Mixed Signal Design & Verification	Paper Session 5A: Design Verification - Scenario Generation/Usage
11:15	11:45	1A1:3195 - Design Implementation of Generic Architecture for Image Processing Applications and its Verification with UVM Framework <i>Sougata Bhattacharjee</i>	2A1:1947 - Navigating Instruction Length Decode: TAP into IP using Formal Verification <i>Vedprakash Mishra</i>	3A1:3687 - Sparking UVM stimulus via state design pattern <i>Debarati Banerjee, Nikhil Singla and Rohit Jindal</i>	4A1:639 - Accelerating Silicon Bug Detection and Optimizing Execution Flow through Intelligent Adaptive Glitch Detectors in AMS Verification <i>Aadhar Sharma, Avinash Chaudhary, Bhavya Shah and Sooraj Sekhar</i>	5A1: 296 - Accelerating Sign-Off Cycles: Automated Scenario Extraction from Large Design Landscapes <i>Gaurav Pratap, Vishal Keswani and Sachin Bansal</i>
11:45	12:15	1A2:9722 - Data-Driven Design for Adaptive Multi-Die SoC. <i>Ankita Roy and Vikrant Kapila</i>	2A3:9864 - Early bird catches the bug - the Arch Formal way <i>Aatreyi Bal, Mahendrawada Sai Kameshwara Rao, Siresha Tulluri and Robert Beers</i>	3A2:7056 - SVRAND – Random Configuration – One class to resolve all parts <i>Kaushal Vala, Krupal Kapadiya, Joseph Bauer and Shyam Sharma</i>	4A2:9609 - ChipGuard : A Robust Automated System to Streamline Design Verification Quality Parameters <i>Giridhar Rangarajan, Jitender Dahiya and Sriram K Sounderrajan</i>	5A2:7316 - Expanding Verification Horizons: OOPs-Enhanced Script-Driven Verification using Auto PSS Gen Utility (APGU). <i>Ashutosh Bisht and Manvendra Singh</i>
12:15	12:45	1A3:4275 - A shift-left approach in Qualification of Digital IPs for SoCs by applying next gen automation and data analytics <i>Hirak Jyoti Chakraborty and Ashutosh Bajpai</i>	2A2:3167 - Towards Rigorous Fairness: Formal Verification of Multi-Level Arbitration through Hierarchical Family Chains <i>Vedprakash Mishra and Keerthi B</i>	3A3:3812 - A Generic Clock UVC for Generating and Testing of High Speed PLL and CDR <i>Dipanshu, Mukesh Gandhi, Amab Ghosh & Parag Lonkar</i>	4A3:9754 - Analog Mixed Signal Verification & Validation Methodology: Bridging the Gap between Pre Silicon Verification and Post Silicon Validation <i>Vidya Timmanagoudar, Marcel Oosterhuis and Steef G</i>	5A3:5557 - Pragmatic use cases of ChatGPT in chip verification <i>Ajeetha Kumari Venkatesan and Hemamalini Sundaram</i>
12:45	13:45	Lunch Break				
13:45	14:15	Posters and Exhibitor Visit				
14:15	15:45	Paper Session 1B: Design & Architecture	Paper Session 2B: Formal Verification	Paper Session 3B: Design Verification - 3D IC/Chiplet	Paper Session 4B: Low Power Design & Verification	Paper Session 5B: Emulation
14:15	14:45	1B1:8189 - Automation of Delay Tuning in TSV aware Heterogeneous 3D Inter-Die memory controller <i>Rahul Laxkar, Ananya Sinha, Naveen Srivastava and Sekhar DanguDubiyam</i>	2B1:2190 - Complexity Conquered: Pioneering Formal Verification Methods for Systolic Controllers in Advanced Computing <i>Sarsij Saurabh, Rahul Dabur, Tuskar Agarwal and Vichal Verma</i>	3B1:407 - Protocol Env: A Dynamic approach to Enable Multi-Protocol UCIe Design Verification <i>Vinit Sheth, Deepak Nagaria and Vikas Makhija</i>	4B1:8500 - Next-Gen Low Power Verification: Empowering Shift-Left Predictive Analysis with Virtual Instrumentation <i>Sachin Bansal, Yi Liu, M.Vaishnavi Reddy, Nupur Gupta, Vishal Keswani and Manish Goel</i>	5B1:3974 - Expedited Gate Level Verification – Unleashing the Potential of Netlist Integrated Emulation Platforms <i>Samhith Kumar Pottam, Vasudeva Reddy Ambati, Rahul S S, Sarang Kalbande, Garima Srivastava and Hyundon Kim</i>
14:45	15:15	1B2:6634 - Voltage Slack Analysis as part of Design Robustness analysis to avoid failures due to voltage variations <i>Anurag Sharma and Savithri Sundareswaran</i>	2B2:7611 - Who watches the watchman? FuSa Verification of DCLS configuration through Formal and Static checks <i>Avinash Pandey, Srobona Mitra Mitra, Sayandeep Sanyal, Sathish Kumar Manickam, Deepak Baranwal and Arunava Dutta</i>	3B2:1272 - Beyond Boundaries: Overcoming Chiplet Verification Challenges <i>Pankaj Singh</i>	4B2:1219 - Signal Integrity Challenges in rail-to-rail Parallel Interfaces designed for MEMS, Automotive & Infotainment Applications <i>Piyush Mishra, Suprbha Kumari and Anuj Gupta</i>	5B2:6678 - Simulated Emulation: Methodology For a Faster Turnaround on Emulation <i>Shalini Maheshwari and Ashok Kumar Bhatt</i>
15:15	15:45	1B3:3720 - Generative AI based RTL code generator <i>Hareesh Perumal S, Ashutosh Bajpai, Kranthi Kiran Gandem and Vishnu Dutt Pathak</i>	2B3:1423 - GenAI Leap in Formal Verification Testplanning <i>Anshul Jain, Karan Rawat and Pradip Prajapati</i>	3B3:7052 - Navigating the Maze: Verifying Multi-Module PHY designs in UCIe Multi-Die Systems <i>K S Prasad Subudhi and Narasimha Babu G V L</i>	4B3:3654 - Power Probe: Addressing Power Noise Signal Integrity Challenges for Wide IO HBM Memories Through Advanced Verification Approach <i>Giridhar Rangarajan, Chethan G B, Bhargava Krishna Venigalla, Akhbhobhya B and Anil Deshpande</i>	5B3:2224 - Unveiling Advance Hybrid Emulation Methodology for Accelerated Android Home Screen Bring-up and System Level Verification at Pre-Silicon <i>Rinkesh Yadav, Vishweswaran Kamran, Sarang Kalbande, Garima Srivastava and Hyundon Kim</i>
15:45	16:00	Tea Break & Networking				
16:00	17:30	Paper Session 1C: System /System C	Paper Session 2C: Formal Verification	Paper Session 3C: Design Verification - Coverage/Performance	Paper Session 4C: Functional Safety / RISC-V	Paper Session 5C: Post Silicon
16:00	16:30	1C1:7510 - Early Architecture Exploration of Multi Die Designs <i>Ranjan Mahajan and Souradeep Guha</i>	2C3:6747 - Enhancing Arbitration Integrity: Formal Verification of Weighted Round Robin Arbiter in High-Performance Graphics <i>Usha Rani Bagadi, Mohit Choradia, Ajay Kumar Kolluri and Vichal Verma</i>	3C1:4372 - Register model back door access automation for a complex IP <i>Kilaru Vamsikrishna, Dhruv Ashvinbhai Donga and Sushrut B Veerapur</i>	4C1:955 - Leveraging Statistical Random Fault (SRF) Sampling for Efficient Functional Safety with reduced efforts <i>Gulshan Kumar Sharma, Sougata Bhattacharjee, Akshaya Kumar Jain, Udaykrishna J, Gaurav Goel and Arun Gogineni</i>	5C1:344 - Video/JPEG Performance Analysis and UseCases Validation in Post Silicon using SystemC and OpenVINO based Neural Network models <i>Suresh Vasu and Palanivel Guruswarediar</i>
16:30	17:00	1C2:9221 - SDV Aware Verification : Verification Challenges , Opportunities & Evolution around SW Defined Vehicles (SDV) & Zonal Architectures <i>Neha Srivastava</i>	2C2:2323 - A Novel Flow for Low-Power Assertion-Based Verification for Improved Quality and Time-to-Market <i>Gurleen Kaur</i>	3C2:5643 - Unified Coverage Methodology: Accelerated Coverage Closure at SoC and IP level <i>Prateek Jain and Ajay Goyal</i>	4C2:9497 - An Extension to RISC-V Test Generator : A quick exception check <i>Ranjan Barik, Sai Krishna Pidugu, Manju Bhargavi and Subhra Kanti Das</i>	5C2:6777 - Enhancing Post-Silicon Validation Through Generative Adversarial Networks (GANs) for Test Case Generation <i>Aditi Bhamaiik and Vidhya Sagar</i>
17:00	17:30	1C3:614 - Early Performance Exploration of Memory based on JEDEC Specifications <i>Parvinder Asija and Aman Gupta</i>	2C3:9882 - Pioneering Software Formal Verification Methodology for Firmware <i>Sparsa Roychowdhury, Disha Puri and Sudipa Mandal</i>	3C3:7227 - Simulation performance improvement with Dynamic memory load & C model export <i>Varsha Antony and Mangesh Kondalkar</i>	4C3:2603 - Verification Methodology for Debug Unit of a Superscalar RISC-V Processor <i>Ajay Sharma, Afshan Anjum and Sourav Roy</i>	5C3:1035 - An Automated approach for optimizing Circuit Marginality Validation methodologies <i>Vivek Sharma, Pankaj Sharma and Subrata Kumar Behera</i>
17:30	18:00	Best Paper Awards & Closing				