Thursday, September 19, 2024

Start	End	Track 1 - Grand Victoria B	Track 2 - Grand Victoria A	Track 3 - Robusta & Arabica	Track 4 - Brain Box	Track 5 - Marquis
09:00	09:15	General Sessions - Grand Victoria				
09:00	09:15	Welcome & TPC Update				
09:15	09:45	Keynote: *Accelerated Infrastructure in an AI World* Puneet Agarwal, Marvell				
09:45	10:15	Keynote: Qualcomm				
10:15	11:00	Industry Panel: Building RISC-V Systems: An Indian Perspective				
11:00	11:15	Tea Break & Networking				
11:15	12:45	Paper Session 1A: Design & Architecture	Paper Session 2A: Formal Verification	Paper Session 3A: Design Verification - SV & UVM	Paper Session 4A: Mixed Signal Design & Verification	Paper Session 5A: Design Verification - Scenario Generation/Usage
11:15	11:45	1A1:3195 - Design Implementation of Generic Architecture for Image Processing Applications and its Verification with UVM Framework *Sougata Bhattacharjee*	2A1:1947 - Navigating Instruction Length Decode: TAP into IP using Formal Verification *Vedprakash Mishra*	3A1:3687 - Sparking UVM stimulus via state design pattern *Debarati Banerjee, Nikhil Singla and Rohit Jindal*	4A1:639 - Accelerating Silicon Bug Detection and Optimizing Execution Flow through Intelligent Adaptive Glitch Detectors in AMS Verification *Aadhar Sharma, Avinash Chaudhary, Bhavya Shah and Sooraj Sekhar*	5A1: 296 - Accelerating Sign-Off Cycles: Automated Scenario Extraction from Large Design Landscapes *Gaurav Pratap, Vishal Keswani and Sachin Bansal*
11:45	12:15	1A2:9722 - Data-Driven Design for Adaptive Multi-Die SoC. *Ankita Roy and Vikrant Kapila*	2A3:9864 - Early bird catches the bug - the Arch Formal way *Aatreyi Bal, Mahendrawada Sai Kameshwara Rao, Sireesha Tulluri and Robert Beers*	3A2:7056 - SVRAND – Random Configuration – One class to resolve all parts *Kaushal Vala, Krunal Kapadiya, Joseph Bauer and Shyam Sharma*	4A2:9609 - ChipGuard : A Robust Automated System to Streamline Design Verification Quality Parameters *Giridhar Rangarajan, Jitender Dahiya and Sriram K Sounderrajan*	5A2:7316 - Expanding Verification Horizons: OOPs-Enhanced Script-Driven Verification using Auto PSS Gen Utility (APGU). *Ashutosh Bisht and Manvendra Singh*
12:15	12:45	1A3:4275 - A shift-left approach in Qualification of Digital IPs for SoCs by applying next gen automation and data analytics *Hirak Jyoti Chakraborty and Ashutosh Bajpai*	2A2:3167 - Towards Rigorous Fairness: Formal Verification of Multi-Level Arbitration through Hierarchical Family Chains *Vedprakash Mishra and Keerthi B*	3A3:3812 - A Generic Clock UVC for Generating and Testing of High Speed PLL and CDR *Dipanshu, Mukesh Gandhi, Arnab Ghosh and Parag S Lonkar*	4A3:9754 - Analog Mixed Signal Verification and Validation(V&V) Methodology: Bridging the Gap between Pre Silicon Verification and Post Silicon Validation *Vidya Timmanagoudar, Marcel Oosterhuis and Steef Grimbergen*	5A3:5557 - Pragmatic use cases of ChatGPT in chip verification *Ajeetha Kumari Venkatesan and Hemamalini Sundaram*
12:45	13:45	Lunch Break				
13:45	14:15	Posters and Exhibitor Visit				
14:15	15:45	Paper Session 1B: Design & Architecture	Paper Session 2B: Formal Verification	Paper Session 3B: Design Verification - 3D IC/Chiplet	Paper Session 4B: Low Power Design & Verification	Paper Session 5B: Emulation
14:15	14:45	1B1:8189 - Automation of Delay Tuning in TSV aware Heterogeneous 3D Inter-Die memory controller *Rahul Laxkar, Ananya Sinha, Naveen Srivastava and Sekhar Dangudubiyyam*	2B1:2190 - Complexity Conquered: Pioneering Formal Verification Methods for Systolic Controllers in Advanced Computing *Sarsij Saurabh, Rahul Dabur, Tushar Agarwal and Vichal Verma*	3B1:407 - Protocol Env: A Dynamic approach to Enable Multi-Protocol UCIe Design Verification *Vinit Sheth, Deepak Nagaria and Vikas Makhija*	4B1:8500 - Next-Gen Low Power Verification: Empowering Shift-Left Predictive Analysis with Virtual Instrumentation *Sachin Bansal, Yi Liu, M.Vaishnavi Reddy, Nupur Gupta, Vishal Keswani and Manish Goel*	5B1:3974 - Expedited Gate Level Verification – Unleashing the Potential of Netlist Integrated Emulation Platforms *Samhith Kumar Pottem, Vasudeva Reddy Ambati, Rahul S S, Sarang Kalbande, Garima Srivastava and Hyundon Kim*
14:45	15:15	1B2:8314 - A Novel Leakage Power Reduction Technique in SRAM Cell in sub-32 nm technologies *Ankit Raj*	2B2:7611 - Who watches the watchman? FuSa Verification of DCLS configuration through Formal and Static checks *Avinash Pandey, Srobona Mitra Mitra, Sayandeep Sanyal, Sathish Kumar Manickam, Deepak Baranwal and Arunava Dutta*	3B2:1272 - Beyond Boundaries: Overcoming Chiplet Verification Challenges *Pankaj Singh*	4B2:1219 - Signal Integrity Challenges in rail-to-rail Parallel Interfaces designed for MEMS, Automotive & Infotainment Applications *Piyush Mishra, Suprbha Kumari and Anuj Gupta*	5B2:6678 - Simulated Emulation: Methodology For a Faster Turnaround on Emulation *Shalini Maheshwari and Ashok Kumar Bhatt*
15:15	15:45	1B3:3720 - Generative AI based RTL code generator *Hareesh Perumal S, Ashutosh Bajpai, Kranthi Kiran Gandem and Vishnu Dutt Pathak*	2B3:1423 - GenAI Leap in Formal Verification Testplanning *Anshul Jain, Karan Rawat and Pradip Prajapati*	3B3:7052 - Navigating the Maze: Verifying Multi-Module PHY designs in UCIe Multi-Die Systems *K S Prasad Subudhi and Narasimha Babu G V L*	4B3:3654 - Power Probe: Addressing Power Noise Signal Integrity Challenges for Wide IO HBM Memories Through Advanced Verification Approach *Giridhar Rangarajan, Chethan G B, Bhargava Krishna Venigalla, Akbhobhya B and Anil Deshpande*	5B3:2224 - Unveiling Advance Hybrid Emulation Methodology for Accelerated Android Home Screen Bring-up and System Level Verification at Pre-Silicon *Rinkesh Yadav, Vishweswaran Kannan, Sarang Kalbande, Garima Srivastava and Hyundon Kim*
15:45	16:00	Tea Break & Networking				
16:00	17:30	Paper Session 1C System/System C	Paper Session 2C Formal Verification	Paper Session 3C Design Verification - Coverage/Performance	Paper Session 4C Functional Safety / RISC-V	Paper Session 5C Post Silicon
16:00	16:30	1C1:7510 - Early Architecture Exploration of Multi Die Designs *Ranjan Mahajan and Souradeep Guha*	2C1:5782 - Formal Verification Framework for Hardware Accelerator Designs *Anmol Patel, Kevin Bhensdadiya and Anshul Jain*	3C1:4372 - Register model back door access automation for a complex IP *Kilaru Vamsikrishna, Dhruv Ashvinbhai Donga and Sushrut B Veerapur*	4C1:955 - Leveraging Statistical Random Fault (SRF) Sampling for Efficient Functional Safety with reduced efforts *Gulshan Kumar Sharma, Sougata Bhattacharjee, Akshaya Kumar Jain, Udaykrishna J, Gaurav Goel and Arun Gogineni*	5C1:344 - Video/JPEG Performance Analysis and UseCases Validation in Post Silicon using SystemC and OpenVINO based Neural Network models *Suresh Vasu and Palanivel Guruvareddiar*
16:30	17:00	IC2:9221 - SDV Aware Verification : Verification Challenges , Opportunities & Evolution around SW Defined Vehicles (SDV) & Zonal Architectures *Neha Srivastava*	2C2:2323 - A Novel Flow for Low-Power Assertion-Based Verification for Improved Quality and Time-to-Market *Gurleen Kaur*	3C2:5643 - Unified Coverage Methodology: Accelerated Coverage Closure at SoC and IP level *Prateek Jain and Ajay Goyal*	4C2:9497 - An Extension to RISC-V Test Generator : A quick exception check *Ranjan Barik, Sai Krishna Pidugu, Manju Bhargavi and Subhra Kanti Das*	5C2:6777 - Enhancing Post-Silicon Validation Through Generative Adversarial Networks (GANs) for Test Case Generation *Aditi Bharmaik and Vidhya Sagar*
17:00	17:30	IC3:614 - Early Performance Exploration of Memory based on JEDEC Specifications *Parvinder Asija and Aman Gupta*	2C3:6747 - Enhancing Arbitration Integrity: Formal Verification of Weighted Round Robin Arbiter in High-Performance Graphics *Usha Rani Bagadi, Mohit Choradia, Ajay Kumar Kolluri and Vichal Verma*	3C3:7227 - Simulation performance improvement with Dynamic memory load & C model export *Varsha Antony and Mangesh Kondalkar*	4C3:2603 - Verification Methodology for Debug Unit of a Superscalar RISCV Processor *Ajay Sharma, Afshan Anjum and Sourav Roy*	5C3:1035 - An Automated approach for optimizing Circuit Marginality Validation methodologies *Vivek Sharma, Pankaj Sharma and Subrata Kumar Behera*
17:30	18:00	Best Paper Awards & Closing				