


Wednesday, September 18, 2024

Start	End	General Sessions - Grand Victoria			
09:15	09:45	DVCon India 2024 Inauguration			
09:45	10:30	Vision Talk: <i>Empowering Innovation: Harnessing Collective Wisdom across Tools, Processes, and People!</i> Harry Foster, Siemens			
10:30	11:15	Industry Panel: <i>Strengthening India's Fab Ecosystem: The Critical Role of the Design Community</i> Moderator: Sumedha Limaye, Intel; Panelists: Ruchir Dixit, IESA; Pradeep CR, Ausdia; Surya Musunuri, Infineon; Venkatesh Narasimhan, Silicon Labs			
11:15	11:30	Tea Break & Networking			
Start	End	Track 1 - Grand Victoria B	Track 2 - Grand Victoria A	Track 3 - Robusta & Arabica	Track 4 - Brain Box
11:30	12:15	Tutorial 1A: Expanding role of Static Signoff in Verification Coverage <i>Vikas Sachdeva, Real Intent</i>	Tutorial 2A: Next Generation Debug <i>Rohit Ohlayan & Prasad Chelur, Synopsys</i>	Short Workshop 3A_1: Find and Fix Excessive Power Dissipation of your Chip Very Early in the Design Cycle <i>Manish Pandey, Siemens</i>	Short Workshop 4A_1: What's new in SystemC 3.0 - IEEE 1666-2023 <i>Aravinda Thimmapuram, CircuitSutra</i>
12:15	13:00			Short Workshop 3A_2: Power Dynamics: Shaping the Future of the Data-Centric Era <i>Vijay Chobisa & Gaurav Saharawat, Siemens</i>	Short Workshop 4A_2: Harnessing AI for Enhanced Verification Efficiency <i>Anika Sunda, Cadence</i>
13:00	14:00	Lunch Break			
14:00	14:30	Keynote: <i>AI for Verification – Today's Reality Vs. Tomorrow's Promisedence</i> Matt Graham, Cadence			
14:30	15:00	Keynote: <i>The Future is Formal</i> Ashish Darbari, Axiomise			
15:15	15:45	Keynote: <i>Navigating the Future of Chip Design Verification in an Era of Rapid Semiconductor Innovation</i> Apurva Kumar, Quest Global			
15:45	16:00	Tea Break & Networking			
16:00	16:45	Tutorial 1B: Bridging the Gap: Standardizing CDC and RDC Closure with Interoperable Abstract Models <i>Accellera</i>	Short Workshop 2B_1: High performance design verification techniques <i>Arun Joseph & Chakrapani Rayadurgam, IBM</i>	Short Workshop 3B_1: Functional Safety and High reliability in FPGA design <i>Nilesh Shilankar & Manohar Reddy Vadicherla, Synopsys</i>	Short Workshop 4B_1: Efficient RISC V Compute Platforms for Enabling the AI Revolution <i>Sujay Deb, IIIT-D for Aarfive Designs</i>
16:45	17:30		Short Workshop 2B_2: Portable Stimulus and VIP: Like a Hand in a Glove <i>Raghavendra HM & Manoj Manu, Siemens</i>	Short Workshop 3B_2: FPGA Prototyping for Large Multi-Die/Multi-Core Designs <i>Madhav Chikodikar & Subhankar Ghosh, Synopsys</i>	Short Workshop 4B_2: Emergence of DIR-V and VEGA Processor Ecosystem <i>Libin TT, CDAC</i>
17:30	17:45	Day 1 Closing Remarks			
17:45	19:00	Networking			
19:00	19:10	DVCon India 2024 Awards Welcome - Tessolve			
19:10	20:00	Leadership Talk: <i>Awake Thyself</i> Arjun Devaiah, International Athlete & National Sprint Champion			
20:00	20:30	DVCon India 2024 Awards			
20:30	22:00	Drinks & Dinner			