Wednesday, September 18, 2024

Start	End	Track 1 - Grand Victoria B	Track 2 - Grand Victoria A	Track 3 - Robusta & Arabica	Track 4 - Brain Box
09:00	09:15	General Sessions - Grand Victoria DVCon India 2024 Inauguration			
09:15	10:00	Vision Talk: *Empowering Innovation: Harnessing Collective Wisdom across Tools, Processes, and People!* Harry Foster,Siemens			
10:00	10:30	Keynote: The Increasing Verification Horizon in the Era of Pervasive Intelligence Vikas Gautam, Synopsys & Subrangshu Das, Google			
10:30	11:15	Industry Panel: Strengthening India's Fab Ecosystem: The Critical Role of the Design Community Moderator: Sumedha Limaye, Intel; Panelists: Ruchir Dixit, IESA; Pradeep CR, Ausdia; Surya Musunuri, Infineon; Venkatesh Narasimhan, Silicon Labs			
11:15	11:30	Tea Break & Networking			
11:30	12:15	Tutorial 1A: Expanding role of Static Signoff in Verification Coverage *Vikas Sachdeva, Real Intent*	Tutorial 2A: Next Generation Debug *Rohit Ohlayan & Prasad Chelur, Synopsys*	Short Workshop 3A_1: Find and Fix Excessive Power Dissipation of your Chip Very Early in the Design Cycle *Manish Pandey, Siemens*	Short Workshop 4A_1: What's new in SystemC 3.0 - IEEE 1666-2023 *Aravinda Thimmapuram, CircuitSutra*
12:15	13:00			Short Workshop 3A_2: Power Dynamics: Shaping the Future of the Data-Centric Era *Vijay Chobisa and Gaurav Saharawat, Siemens*	Short Workshop 4A_2: Harnessing AI for Enhanced Verification Efficiency *Anika Sunda, Cadence*
13:00	14:00	Lunch Break			
14:00	14:30	Keynote: AI for Verification – Today's Reality Vs. Tomorrow's Promisedence Matt Graham, Cadence			
14:30	15:00	Keynote: The Future is Formal Ashish Darbari, Axiomise			
15:15	15:45	Keynote: Navigating the Future of Chip Design Verification in an Era of Rapid Semiconductor Innovation Apurva Kumar, Quest Global			
15:45	16:00	Tea Break & Networking			
16:00	16:45	Tutorial 1B: Bridging the Gap: Standardizing CDC and RDC Closure with Interoperable Abstract Models *Accellera*	Short Workshop 2B_1: High performance design verification techniques *Arun Joseph and Puja Sethia, IBM*	Short Workshop 3B_1: Functional Safety and High reliability in FPGA design *Nilesh Shilankar and Manohar Reddy Vadicherla, Synopsys*	Short Workshop 4B_1: RISC- V adoption in India *Priyanka Das, Aarfive*
16:45	17:30		Short Workshop 2B_2: Portable Stimulus and VIP: Like a Hand in a Glove *Pradeep Salla, Raghavendra HM, Siemens*	Short Workshop 3B_2: FPGA Prototyping for Large Multi-Die/Multi-Core Designs *Madhav Chikodikar and Subhankar Ghosh, Synopsys*	Short Workshop 4B_2: RISC-V Ecosystem *Libin T T, CDAC*
17:30	17:45	Day 1 Closing Remarks			
17:45	19:00	Networking			
19:00	19:10	DVCon India 2024 Awards Welcome - Tessolve			
19:10	20:00	Leadership Talk: Awake Thyself Arjun Devaiah, International Athlete & National Sprint Champion			
20:00	20:30	DVCon India 2024 Awards			
20:30	22:00	Drinks & Dinner			