

Wednesday, September 18, 2024



Start	End	General Sessions - Grand Victoria			
09:15	09:45	DVCOn India 2024 Inauguration			
09:45	10:30	Vision Talk: <i>Empowering Innovation: Harnessing Collective Wisdom across Tools, Processes, and People!</i> Harry Foster, Siemens			
10:30	11:15	Industry Panel: Strengthening India's Fab Ecosystem: The Critical Role of the Design Community Moderator: Sumedha Limaye, Intel; Panelists: Ruchir Dixit, IESA; Pradeep CR, Ausdia; Surya Musunuri, Infineon; Venkatesh Narasimhan, Silicon Labs			
11:15	11:30	Tea Break & Networking			
Start	End	Track 1 - Grand Victoria B	Track 2 - Grand Victoria A	Track 3 - Robusta & Arabica	Track 4 - Brain Box
11:30	12:15	Tutorial 1A:	Tutorial 2A:	Short Workshop 3A_1:	Short Workshop 4A_1:
12:15	13:00			Short Workshop 3A_2:	Short Workshop 4A_2:
13:00	14:00	Lunch Break			
14:00	14:30	Keynote: AI for Verification – Today's Reality Vs. Tomorrow's Promisedence Matt Graham, Cadence			
14:30	15:00	Keynote: The Future is Formal Ashish Darbari, Axiomise			
15:15	15:45	Keynote: Navigating the Future of Chip Design Verification in an Era of Rapid Semiconductor Innovation Apurva Kumar, Quest Global			
15:45	16:00	Tea Break & Networking			
16:00	16:45	Tutorial 1B:	Short Workshop 2B_1:	Short Workshop 3B_1:	Short Workshop 4B_1:
16:45	17:30		Short Workshop 2B_2:	Short Workshop 3B_2:	Short Workshop 4B_2:
17:30	17:45	Day 1 Closing Remarks			
17:45	19:00	Drinks & Networking			
19:00	19:10	DVCOn India 2024 Awards Welcome - Tessolve			
19:10	20:00	Leadership Talk: <i>Awake Thyself</i> Arjun Devaiah, International Athlete & National Sprint Champion			
20:00	20:30	DVCOn India 2024 Awards			
20:30	22:00	Dinner			

Exhibit Areas

EXHIBIT HOURS
11:00am to 7pm

Thursday, September 19, 2024



Start	End	General Sessions - Grand Victoria					
09:00	09:15	Welcome & TPC Update					EXHIBIT HOURS 9am to 6pm
09:15	09:45	Keynote: <i>Accelerated Infrastructure in an AI World</i> Puneet Agarwal, Marvell					
09:45	10:15	Keynote: The Increasing Verification Horizon in the Era of Pervasive Intelligence Vikas Gautam, Synopsys & Subrangshu Das, Google					
10:15	11:00	Industry Panel: Building RISC-V Systems: An Indian Perspective Moderator: Subhra Kanti Das, Thales Panelists: Dr. Krishna Kumar Rao, CDAC; Sundar Haran, Western Digital; Srikanth Puvvada, Ola-Krutrim; Neel Gala, Incore Semiconductor					
11:00	11:15	Tea Break & Networking					POSTER HOURS 11:00am to 4:30pm
Start	End	Track 1 - Grand Victoria B	Track 2 - Grand Victoria A	Track 3 - Robusta & Arabica	Track 4 - Brain Box	Track 5 - Marquis	
11:15	12:45	Paper Session 1A: Design & Architecture	Paper Session 2A: Formal Verification	Paper Session 3A: Design Verification - SV & UVM	Paper Session 4A: Mixed Signal Design & Verification	Paper Session 5A: Scenario Generation/Usage	
11:15	11:45	1A1:	2A1:	3A1:	4A1:	5A1:	
11:45	12:15	1A2:	2A2:	3A2:	4A2:	5A2:	
12:15	12:45	1A3:	2A3:	3A3:	4A3:	5A3:	
12:45	13:45	Lunch Break					
13:45	14:15	Posters and Exhibitor Visit					
14:15	15:45	Paper Session 1B: Design & Architecture	Paper Session 2B: Formal Verification	Paper Session 3B: 3DIC/Chiplet	Paper Session 4B: Low Power Design & Verif	Paper Session 5B: Emulation	
14:15	14:45	1B1:	2B1:	3B1:	4B1:	5B1:	
14:45	15:15	1B2:	2B2:	3B2:	4B2:	5B2:	
15:15	15:45	1B3:	2B3:	3B3:	4B3:	5B3:	
15:45	16:00	Tea Break & Networking					
16:00	17:30	Paper Session 1C: System/System C	Paper Session 2C: Formal Verification	Paper Session 3C: Coverage/Performance	Paper Session 4C: Functional Safety / RISC-V	Paper Session 5C: Post Silicon	
16:00	16:30	1C1:	2C1:	3C1:	4C1:	5C1:	
16:30	17:00	1C2:	2C2:	3C2:	4C2:	5C2:	
17:00	17:30	1C2:	2C3:	3C3:	4C3:	5C3:	
17:30	18:00	Best Paper Awards & Closing					