

DVCOn India 2024: Selected Papers List

Paper Session 1A: Design & Architecture

1A1:3195 - Design Implementation of Generic Architecture for Image Processing Applications and its Verification with UVM Framework

Sougata Bhattacharjee, SAMSUNG

1A2:9722 - Data-Driven Design for Adaptive Multi-Die SoC.

Ankita Roy and Vikrant Kapila, INTEL

1A3:4275 - A shift-left approach in Qualification of Digital IPs for SoCs by applying next gen automation and data analytics

Hirak Jyoti Chakraborty and Ashutosh Bajpai, INFINEON

Paper Session 1B: Design & Architecture

1B1:8189 - Automation of Delay Tuning in TSV aware Heterogeneous 3D Inter-Die memory controller

Rahul Laxkar, Ananya Sinha, Naveen Srivastava and Sekhar Dangudubiyam, SAMSUNG

1B2:6634 - Voltage Slack Analysis as part of Design Robustness analysis to avoid failures due to voltage variations

Anurag Sharma and Savithri Sundareswaran

1B3:3720 - Generative AI based RTL code generator

Hareesh Perumal S, Ashutosh Bajpai, Kranthi Kiran Gandem and Vishnu Dutt Pathak, INFINEON

Paper Session 1C System/System C

1C1:7510 - Early Architecture Exploration of Multi Die Designs

Ranjan Mahajan and Souradeep Guha, SYNOPSIS

1C2:9221 - SDV Aware Verification: Verification Challenges , Opportunities & Evolution around SW Defined Vehicles (SDV) & Zonal Architectures

Neha Srivastava, NXP

1C3:614 - Early Performance Exploration of Memory based on JEDEC Specifications

Parvinder Asija and Aman Gupta, SYNOPSIS

Paper Session 2A: Formal Verification

2A1:1947 - Navigating Instruction Length Decode: TAP into IP using Formal Verification

Vedprakash Mishra, INTEL

2A3:9864 - Early bird catches the bug - the Arch Formal way

Aatreyi Bal, Mahendrawada Sai Kameshwara Rao, Sireesha Tulluri and Robert Beers, INTEL

2A2:3167 - Towards Rigorous Fairness: Formal Verification of Multi-Level Arbitration through Hierarchical Family Chains

Vedprakash Mishra and Keerthi B, INTEL

Paper Session 2B: Formal Verification

2B1:2190 - Complexity Conquered: Pioneering Formal Verification Methods for Systolic Controllers in Advanced Computing

Sarsij Saurabh, Rahul Dabur, Tushar Agarwal and Vichal Verma, INTEL

2B2:7611 - Who watches the watchman? FuSa Verification of DCLS configuration through Formal and Static checks

Avinash Pandey, Srobona Mitra Mitra, Sayandeep Sanyal, Sathish Kumar Manickam, Deepak Baranwal and Arunava Dutta, QUALCOMM

2B3:1423 - GenAI Leap in Formal Verification Testplanning

Anshul Jain, Karan Rawat and Pradip Prajapati, INTEL

Paper Session 2C: Formal Verification

2C1:6747 - Enhancing Arbitration Integrity: Formal Verification of Weighted Round Robin Arbiter in High-Performance Graphics

Usha Rani Bagadi, Mohit Choradia, Ajay Kumar Kolluri and Vichal Verma, INTEL

2C2:7372 - Efficiently Analyzing Unreachable Properties in Configuration-Based Designs with Automated Mode-Aware Coverage Analysis

Vedprakash Mishra and Shravya Jampana, INTEL

2C3:9882 - Pioneering Software Formal Verification Methodology for Firmware

Sparsa Roychowdhury, Disha Puri and Sudipa Mandal, INTEL

Paper Session 3A: Design Verification - SV & UVM

3A1:3687 - Sparking UVM stimulus via state design pattern

Debarati Banerjee, Nikhil Singla and Rohit Jindal, GOOGLE

3A2:7056 - SVRAND – Random Configuration – One class to resolve all parts

Kaushal Vala, Krunal Kapadiya, Joseph Bauer and Shyam Sharma, CADENCE

3A3:3812 - A Generic Clock UVC for Generating and Testing of High Speed PLL and CDR

Dipanshu, Mukesh Gandhi, Arnab Ghosh and Parag S Lonkar, SAMSUNG

Paper Session 3B: Design Verification - 3D IC/Chiplet

3B1:407 - Protocol Env: A Dynamic approach to Enable Multi-Protocol UCle Design Verification

Vinit Sheth, Deepak Nagaria and Vikas Makhija, SYNOPSYS

3B2:1272 - Beyond Boundaries: Overcoming Chiplet Verification Challenges

Pankaj Singh, CADENCE

3B3:7052 - Navigating the Maze: Verifying Multi-Module PHY designs in UCle Multi-Die Systems

K S Prasad Subudhi and Narasimha Babu G V L, SYNOPSYS

Paper Session 3C: Design Verification - Coverage/Performance

3C1:4372 - Register model back door access automation for a complex IP

Kilaru Vamsikrishna, Dhruv Ashvinbhai Donga and Sushrut B Veerapur, CADENCE

3C2:5643 - Unified Coverage Methodology: Accelerated Coverage Closure at SoC and IP level

Prateek Jain and Ajay Goyal, SYNOPSYS

3C3:7227 - Simulation performance improvement with Dynamic memory load & C model export

Varsha Antony and Mangesh Kondalkar, QUALCOMM

Paper Session 4A: Mixed Signal Design & Verification

4A1:639 - Accelerating Silicon Bug Detection and Optimizing Execution Flow through Intelligent Adaptive Glitch Detectors in AMS Verification

Aadhar Sharma, Avinash Chaudhary, Bhavya Shah and Sooraj Sekhar, TI

4A2:9609 - ChipGuard : A Robust Automated System to Streamline Design Verification Quality Parameters

Giridhar Rangarajan, Jitender Dahiya and Sriram K Sounderrajan, SAMSUNG

4A3:9754 - Analog Mixed Signal Verification and Validation(V&V) Methodology: Bridging the Gap between Pre Silicon Verification and Post Silicon Validation

Vidya Timmanagoudar, Marcel Oosterhuis and Steef Grimbergen, NXP

Paper Session 4B: Low Power Design & Verification

4B1:8500 - Next-Gen Low Power Verification: Empowering Shift-Left Predictive Analysis with Virtual Instrumentation

Sachin Bansal, Yi Liu, M.Vaishnavi Reddy, Nupur Gupta, Vishal Keswani and Manish Goel, SYNOPSIS

4B2:1219 - Signal Integrity Challenges in rail-to-rail Parallel Interfaces designed for MEMS, Automotive & Infotainment Applications

Piyush Mishra, Suprbha Kumari and Anuj Gupta, STMicroelectronics

4B3:3654 - Power Probe: Addressing Power Noise Signal Integrity Challenges for Wide IO HBM Memories Through Advanced Verification Approach

Giridhar Rangarajan, Chethan G B, Bhargava Krishna Venigalla, Akbhobhya B and Anil Deshpande, SAMSUNG

Paper Session 4C: Functional Safety / RISC-V

4C1:955 - Leveraging Statistical Random Fault (SRF) Sampling for Efficient Functional Safety with reduced efforts

Gulshan Kumar Sharma, Sougata Bhattacharjee, Akshaya Kumar Jain, Udaykrishna J, Gaurav Goel and Arun Gogineni, SAMSUNG & SIEMENS

4C2:9497 - An Extension to RISC-V Test Generator: A quick exception check

Ranjan Barik, Sai Krishna Pidugu, Manju Bhargavi and Subhra Kanti Das, THALES GROUP

4C3:2603 - Verification Methodology for Debug Unit of a Superscalar RISC-V Processor

Ajay Sharma, Afshan Anjum and Sourav Roy, NXP

Paper Session 5A: Design Verification - Scenario Generation/Usage

5A1:296 - Accelerating Sign-Off Cycles: Automated Scenario Extraction from Large Design Landscapes

Gaurav Pratap, Vishal Keswani and Sachin Bansal, SYNOPSYS

5A2:7316 - Expanding Verification Horizons: OOPs-Enhanced Script-Driven Verification using Auto PSS Gen Utility (APGU).

Ashutosh Bisht and Manvendra Singh, STMicroelectronics

5A3:5557 - Pragmatic use cases of ChatGPT in chip verification

Ajeetha Kumari Venkatesan and Hemamalini Sundaram, VERIFWORKS

Paper Session 5B: Emulation

5B1:3974 - Expedited Gate Level Verification – Unleashing the Potential of Netlist Integrated Emulation Platforms

Samhith Kumar Pottem, Vasudeva Reddy Ambati, Rahul S S, Sarang Kalbande, Garima Srivastava and Hyundon Kim, SAMSUNG

5B2:6678 - Simulated Emulation: Methodology For a Faster Turnaround on Emulation

Shalini Maheshwari and Ashok Kumar Bhatt, SYNOPSYS

5B3:2224 - Unveiling Advance Hybrid Emulation Methodology for Accelerated Android Home Screen Bring-up and System Level Verification at Pre-Silicon

Rinkesh Yadav, Vishweswaran Kannan, Sarang Kalbande, Garima Srivastava and Hyundon Kim, SAMSUNG

Paper Session 5C: Post Silicon

5C1:344 - Video/JPEG Performance Analysis and UseCases Validation in Post Silicon using SystemC and OpenVINO based Neural Network models

Suresh Vasu and Palanivel Gurusvareddiar, INTEL

5C2:6777 - Enhancing Post-Silicon Validation Through Generative Adversarial Networks (GANs) for Test Case Generation

Aditi Bharmalik and Vidhya Sagar, INTEL

5C3:1035 - An Automated approach for optimizing Circuit Marginality Validation methodologies

Vivek Sharma, Pankaj Sharma and Subrata Kumar Behera, INTEL