DVCon India 2026
Selected Papers List - Day 1 Conference

Paper Session 1A: SV & UVM / AI
1A1: AI-Augmented Constrained Randomized Framework with Feature-Specific Dynamic Customization for Lpddr6 based design Verification Coverage - by Dharini Subashchandran, Gruheshkumar Patel, Meghna Ahuja and Shyam Sharma
1A2: AI Enabled Portable Stimulus Standard: Bridging the Gap Between Specification and Validation - by Kashish Jangid, Kaushal Modi and Ponnambalam Lakshmanan
1A3: LLM-Guided Closed-Loop Framework Development for Regression Reduction - by Aastha Sanjay Bhore, Arun Joseph and Binod Kumar

Paper Session 1B: SV & UVM / AI
1B1: AI Driven Regression Optimization and Coverage Closure with Cadence Verisium SimAI - by Vishnu G, Aravind R K, Krishna Priyanka Immidisetti and Sahadev Kumar
1B2: Navigating the Cutting Edge: Strategic Verification of UFS 5.0 in Next-Gen AI SoCs - by Premkumar Dhanabalan, Harsha Gollapalli, Shubham Garg, Shyam Sundar, Amitkumar Gound, Akshay R, Srinivasan T and Nikhil Sharma
1B3: NaSTR : Natural language specification to RTL Testbench generation with RAG models - by Ramya B T

Paper Session 2A: Static & Formal
2A1: Control-Datapath Fusion: A Closed-Loop Formal Verification Case Study on Tensor Pipeline Architecture - by Shravya Jampana and Usha Rani Bagadi
2A2: Small Decomposition, Big Payoff: A Case Study on AI-Assisted Formal Verification of a Pipeline Intensive Retry Logic - by Sachin Kumawat, Arjun Singh and Amber Telfer
2A3: Spec to Bug Evidence: An Agentic AI Framework Accelerating Formal Verification Bug Discovery - by Devansh Shah, Neha Joshi and Anshul Jain

Paper Session 2B: Static & Formal
2B1: AI Agents for Data-Driven Reset Abstraction Decisions to Accelerate Formal Proof Convergence - by Anshul Jain, S R Pavitra, Sharika Shaju and Neha Joshi
2B2: FloatFix: An Agentic AI Debugger for Floating-Point Arithmetic in Formal Equivalence Verification - by Suraj Kamble, Mohit Choradia and Vichal Verma
2B3: Next-Gen Firmware Trust: Built on Formal, Scaled with AI - by Disha Puri, Aatreyi Bal and Sudipa Mandal

Paper Session 3A: AMS & Low Power Design
3A1: Porting MBIST and SCAN Testbenches to Chip-Level in Analog-On-Top Designs: Enhancing DFT and Gate-Level Simulations - by Saranya Das
3A2: Left-Shift Power Estimation in SoC Design : Verification-Integrated Framework for Early Power Estimation Using Digital Mixed-Signal Simulation - by Isha Sharma and Amit Singh
3A3: Power Sensitive Mixed-Signal Boundary Elements - by Pankaj Gairola, Anusriti Choudhuri and Serge Garcia-Sabiro

Paper Session 3B: AMS & Low Power Design
3B1: SpecPro Modeller: An AI-Driven Framework for Automated Analog Behavioural Model Generation - by Sainath Karlapalem, Atish Savale and Vihan Shukla
3B2: Beyond Static Analysis: Improving Functional Coverage in Low Power Design Verification - by Arunav Goel, Sachin Bansal, M.Vaishnavi Reddy, Vishal Keswani and Manish Goel
3B3: Design-Focused Feedforward Behavioural Modeling of PLL IPs for Fast SoC Verification - by Preeti Shukla and Amit Singh

Paper Session 4A: Design Architecture
4A1: Task Aware Object Selection using Scene context Reasoning on Edge Hardware - by Avantika Somasundara Kumar Padma Devi, Adlin Rishana J and Shri Varshni N
4A2: The Tokens You Don't Need: Exploiting Video Compression for Faster VLM Inference - by Venkata Ajay Kolla and Suresh Vasu
4A3: Partition of large scale datacenter PCIe subsystem for faster turnaround and partition reusability - by Suraj Augustine, Sathish Sivakumar, Atul Chauhan, Ankush Nehra, Shibin Bose Kavara, Venkatesh Veluvolu, Akhil Goel and Rajat Verma

Paper Session 4B: Design Architecture
4B1: Automated RTL Design Review driven by Microarchitectural Analysis - by Prakash Narain and Vinod Viswanath
4B2: Execution-Aware DRAM Scheduling for Memory-Subsystem Energy Reduction in Near-Memory AI Accelerators - by Vinayak Venkappa Pujeri and Santosh Hanamappa Mokashi
4B3: Low-Power CNN Hardware Accelerator for Real-Time ECG Arrhythmia Detection Using Approximate Multipliers on Zynq FPGA - by Radhakrishnan K R, Ramesh J, Meiyarasan R, Varshaa R and Priyanka D

Paper Session 5A: Functional Safety & Security
5A1: Beyond Syntax: Ensuring the Safety and Style of AI-Generated Hardware - by Amarnath D
5A2: RTL-Centric Safety Verification, A Staged Fault Injection Methodology from FMEDA to System-Level Sign-off Using Simulation and Emulation - by Kiran Maturu, Vedant Garg, Meera Ramani-Augustin, Alex Yap, Pritheshwar Thirugnanasambantham, Rohit Kumar and Lassaad Letaief
5A3: A Methodology for Adversarial and Systematic Concurrency-Aware Security Verification for Memory Protection of MPU/IOMMU Subsystems - by Sridhar Mukund, Prof Sastry Puranapanda, Hemalatha Munnurukapu and Lakshya Panwar

Paper Session 5B: Functional Safety & Security
5B1: Bridging the Gap: A Systematic Verification and Reliability Framework for Analog Compute-in-Memory Using GenAI-Driven Portable Stimulus - by Amarnath D
5B2: Securing Silicon from Birth: Preventing Zero-Fusing Attacks through Lifecycle-Aware Debug Verification - by Sourabh Tapas and Sreedhar Sankaramanchi
5B3: On Security Signoff Experience at RTL driven by Minimally Boolean Static Analysis - by Vinod Viswanath and Varun Sharma

Selected Papers List - Day 2 Conference

Paper Session 1C: SV & UVM / AI
1C1: ML-Driven Automated Functional Verification Framework for Digital Designs - by Laxmikant Chavan and Dr Madhura R
1C2: FunCovr.ai: AI that Generates Sharper Coverage & Smarter Closure - by Mahesh Shinde, Shashivardhan N A, Avinash Anantharamu, Nitin Neralkar and Veeraraju Potta
1C3: Deterministic Generative AI Framework for Context-Aware Verification Testbench Generation - by Govarthanam Krishnasamy

Paper Session 1D: SV & UVM / Debug
1D1: From Prompt to Probe: Left-Shifting SoC Debug with Generative AI - by Gaurang Goyal, Ravi Mangal, Debraj Dutta and Jaideep Ramesh
1D2: CoCorA : An efficient RTL Code debug and Correction Assistant - by Ramya B T
1D3: CLOSED-LOOP DEBUG AGENT: SIMULATION-GATED JOURNAL CONFIRMATION - by Atif Afzal and Meras Pillai Rashid

Paper Session 2C: Static & Formal
2C1: Autonomous Formal Sign-off: Scaling High-Radix Crossbars Verification via GenAI and RPD Synthesis - by Aman Vyas and Nitin Ahuja
2C2: Debug Assist: An LLM-Guided Framework for Debugging FPV Failures - by Kevin Bhensdadiya, Vichal Verma and Ajay Kumar Kolluri
2C3: FUSIOn: Formal verification Using Spec-aware Integration for Optimization - by Bhanu Pratap Singh, Moola Jeevan Chaitanya Goud and Sakthivel Ramaiah

Paper Session 2D: Chiplet Verification
2D1: Multi Die Verificaiton Flow and Methodology - A case study - by Venkata Markandeyulu Boddu
2D2: Agentic AI-Driven UCIe IIP-VIP Integration: Accelerating Chiplet Verification - by Divya Jindal
2D3: Taming AXI Complexity over UCIe: Beyond Protocol Compliance with a Scalable, Configuration-Driven Verification Framework - by Gunjan Kumar Gupta, Sandeep Kumar Chintala, Venkatesh Kudumula, Tai-Jhou Chen and Ray Varghese

Paper Session 3C: SV & UVM
3C1: Analytical Framework for Optimal Sample Point Delay Calculation for Signal I/O Buffers - by Arpit Saxena, Gaurav Jain, Dharini Subashchandran and Shyam Sharma
3C2: FirmScope: Post-Simulation Firmware Debug from Waveforms, PC Traces, and Source Code - by Pradeepkumar Santdasani, Prashant Sharma and Digvijaya Singh
3C3: Reimagining Design Verification: Skilling up the game - by Yaswani Priyanka Vempali and Rajiv Hasija

Paper Session 3D: SV & UVM
3D1: Accelerated verification sign-off: Delta code review and Incremental Coverage Workflow using Synopsys RTL-TRACE - by Bholendra Pratap Singh, Garima Singh and Aravind R K
3D2: Software-Informed Constrained Random Testing: Bridging HW/SW Co-Design and Verification via Temporal Workload Signatures - by Amarnath D
3D3: Verification-Driven Interface Convergence: Methodology for Validating Functional Interoperability And Accelerating Subsystem Design for Concurrently Developed Compute and Component IPs in Coherent Subsystems - by Alisha Parvez, Preethi Ashok Kumar, Shreya Singh, Jyothi Kumari and Rohit Jindal

Paper Session 4C: RISC V Design & Verification
4C1: Directed Adaptive Stimulus Evolution (DASE): Coverage-Directed Evolutionary Stimulus Generation for RISC-V RTL Verification - by Ankush Kumar Jaiswal, Aarav Sharma, Garvit Maheshwari and Jean Jenifer Nesam
4C2: System-Level Verification of N-Trace for a Family of RISC-V Cores - by Nikhil Jain, Kshitij Sukhwal, Jay Gamoneda and Sourav Roy
4C3: Reconfigurable Automated SVA Generator for DFT Validation - by Hemanth Sekhar Kothapalli, Adithya Rangan Ck, Murugeswaran Surulivel, Sivasaravanan R and Kali Mani S

Paper Session 4D: RISC V Design & Verification
4D1: Edge-Efficient Context-Aware Object Detection - by Poojaa Sri S, Rishivathen C and Abishek S
4D2: AI-Driven Coverage-Directed Smoke Regression Optimization via Greedy Set Cover for RISC-V Verification - by Anish Jaltare, Abhishek Rajgadia, Shubham Singla and Radha Govindaradjou
4D3: AI-Driven RTL Change-Aware Testlist Generation for RISC-V Core Verification - by Vikas Dubey, Abhishek Rajgadia, Shubham Singla and Radha Govindaradjou

Paper Session 5C: Emulation/FPGA
5C1: Accelerating GPU Subsystem Verification via Cross Platform Emulation-to-Simulation Trace Replay - by Sanjana Pisal and Rohit Mundada
5C2: SimXL + Gate Level Emulation (GLE): A Validation Technique for Left-Shifting DFT/RTL Bug Discovery in Scandump - by Amita Tekwani, Vijayprasanth V, Naveen Tumati, Rahul Chandran and Pradeep Chandra Akkinapalli
5C3: Adaptive switching between Free-Running and Cycle-Accurate Mode to get high performance and predictive result for Emulation Platform - by Saurabh Shrivastava and Yogesh Mishra

Paper Session 5D: Virtual Prototyping
5D1: LLM-VPBench: An Open Benchmark Suite for Evaluating LLM-Aided SystemC TLM-2.0 Virtual Platform Generation - by Subrat Katiyar and Mahantesh Danagouda
5D2: Optimizing Chiplet based AI subsystems using UCIe and HBM4 TLM models - by Parvinder Kaur, Khushboo Mittal, Vishal Kumar and Priyanshu Suman
5D3: Trace-Driven Software Performance Exploration Using Virtual Platform Architecture for Heterogeneous Automotive ECU Systems - by Bijendra Singh and Soniya Gupta