DVCon India 2026
Selected Posters List

Poster 1: Accelerating Netlist Verification with Debug-Ready Gate-Level Emulation

Authors: Vivek Tiwari and Aravind R K

Poster 2: AI-Assisted Regression Optimization and Coverage Closure Using Synopsys VSO.AI for Complex IP Development

Authors: Vishnu G, Aravind R K, Krishna Priyanka Immidisetti and Bilal Adnan Farooqui

Poster 3: Automation of Structural Code Coverage Exclusions using NPI Driven Programmable Framework for Large Scale NoC Verification

Authors: Nitin Garg

Poster 4: AI/ML-Driven Regression Optimization and Coverage Closure: A Multi-Project Case Study

Authors: Harikrishnan Ananthanarayanan and Prashantkumar Ravindra

Poster 5: Automated Connected Signal Exclusion: Scaling Toggle Coverage Closure in Highly Parameterized IP Verification

Authors: Suresh Kumar Varanasi

Poster 6: PPA_CoPilot: An Agentic Framework for RTL Quality Analysis and PPA Optimization

Authors: Srinivasa Sudhakar Tipparaju

Poster 7: A Modular Architecture for Transport-Independent NVMe Verification and Test Reuse

Authors: Rajan Jani, Darshan Mehta and Vishal Patel

Poster 8: Pre-Silicon Verification of Multi-Vendor UCIe Interoperability: An AI-Enhanced PHY-Centric Methodology

Authors: Ashutosh Singh, K S Prasad Subudhi and Vikas Makhija

Poster 9: A Multiplatform Verification Framework for Automotive 10BaseT Ethernet SoCs

Authors: Bipul Halder, Asjad Fahmi, Sahana S and Krunal Patel

Poster 10: Intelligent RAL: Enhancing UVM Register Abstraction Layer with Built-in Configuration Validation and Coverage

Authors: Sivamanikandan Meenakshi Sundaram and Vinay Datta

Poster 11: AI ASSITED CDC ASSERTION ANALYSIS AND CLASSIFICATION

Authors: Sai Bharadwaj Govindarajula V S, Shanu Kumar Singh, Krishna Priyanka Immidisetti and Aravind R K

Poster 12: Beyond Compliance: A Callback-Driven Fault Injection Methodology for Verifying PCIe Gen6/Gen7 Error Handling and Recovery Mechanisms

Authors: Aneerban Roy, Shafnas K M and Deepak Reddivari

Poster 13: Level4 Virtual Platform for Multi-Die Software Integration and Validation

Authors: Asiful Haque Mondal, Akshata Hosamani and Rupachandra Boggala

Poster 14: SIMD-Based Parallel Data Transfer for Low-Latency Systolic Array Acceleration in AI Workloads

Authors: Yajjala Kumari and Arun Nath K S

Poster 15: Enabling Rapid Hardware Development for Scalable XR Applications Using a Unified Co Simulation Verification Framework

Authors: Azhar Ahammad S K, Arun Magha Rajha Kv, Aman Dhammani and Akshay Jain

Poster 16: Catching the Uncatchable: SDC, CDC, RDC & Glitch Aware RTL Simulation methodology

Authors: Madhav Boddhapu and Pandithurai Sangaiyah

Poster 17: LLM-Based Coverage Waiver: AI-Driven Verification Acceleration

Authors: Uday Kumar Chittireddy

Poster 18: SpecTLB: Design and Development of a Configurable TLB Access Architecture for Speculative Loads in Out-Of-Order Processors

Authors: Jeswin Joseph, Sreelakshmi Pavithran, Libin T T, Divya D S and Krishnakumar Rao

Poster 19: A Lightweight SystemC Profiler for Context Switching Bottlenecks

Authors: Abhay Pratap, Ashwani Aggarwal and Simranjit Singh

Poster 20: Lightweight Custom ISA-Extended Secure Memory Subsystem for PicoRV32 RISC-V With AES Acceleration and Side-Channel Resilience

Authors: Koushik B, Ridhu Pharan A and Mohankumar N

Poster 21: Verification of UCIe Manageability Multi-Chiplet Systems: A Unified and Scalable UVM Methodology

Authors: Sushant Pathak, Deepak Nagaria, Vikas Makhija, Nagesh Mirgane and Nitesh Kumar

Poster 22: AI2: Accelerating Hardware Verification Through Intelligent Automation and Semantic Reasoning

Authors: Hardik Raina

Poster 23: Zero-Vulnerability Low-Power Verification: An Autonomous, Generic Framework for Eliminating Clock and Power Gating Bug Escapes

Authors: Debarati Banerjee and Nikhil Singla