DVCon India 2026
Selected Posters List

Poster 1: Automation of Structural Code Coverage Exclusions using NPI Driven Programmable Framework for Large Scale NoC Verification

Authors: Nitin Garg

Poster 2: A Modular Architecture for Transport-Independent NVMe Verification and Test Reuse

Authors: Rajan Jani, Darshan Mehta and Vishal Patel

Poster 3: Pre-Silicon Verification of Multi-Vendor UCIe Interoperability: An AI-Enhanced PHY-Centric Methodology

Authors: Ashutosh Singh, K S Prasad Subudhi and Vikas Makhija

Poster 4: A Multiplatform Verification Framework for Automotive 10BaseT Ethernet SoCs

Authors: Bipul Halder, Asjad Fahmi, Sahana S and Krunal Patel

Poster 5: Intelligent RAL: Enhancing UVM Register Abstraction Layer with Built-in Configuration Validation and Coverage

Authors: Sivamanikandan Meenakshi Sundaram and Vinay Datta

Poster 6: AI ASSITED CDC ASSERTION ANALYSIS AND CLASSIFICATION

Authors: Sai Bharadwaj Govindarajula V S, Shanu Kumar Singh, Krishna Priyanka Immidisetti and Aravind R K

Poster 7: Beyond Compliance: A Callback-Driven Fault Injection Methodology for Verifying PCIe Gen6/Gen7 Error Handling and Recovery Mechanisms

Authors: Aneerban Roy, Shafnas K M and Deepak Reddivari

Poster 8: Level4 Virtual Platform for Multi-Die Software Integration and Validation

Authors: Asiful Haque Mondal, Akshata Hosamani and Rupachandra Boggala

Poster 9: Enabling Rapid Hardware Development for Scalable XR Applications Using a Unified Co Simulation Verification Framework

Authors: Azhar Ahammad S K, Arun Magha Rajha Kv, Aman Dhammani and Akshay Jain

Poster 10: Catching the Uncatchable: SDC, CDC, RDC & Glitch Aware RTL Simulation methodology

Authors: Madhav Boddhapu and Pandithurai Sangaiyah

Poster 11: LLM-Based Coverage Waiver: AI-Driven Verification Acceleration

Authors: Uday Kumar Chittireddy

Poster 12: SpecTLB: Design and Development of a Configurable TLB Access Architecture for Speculative Loads in Out-Of-Order Processors

Authors: Jeswin Joseph, Sreelakshmi Pavithran, Libin T T, Divya D S and Krishnakumar Rao

Poster 13: A Lightweight SystemC Profiler for Context Switching Bottlenecks

Authors: Abhay Pratap, Ashwani Aggarwal and Simranjit Singh

Poster 14: Lightweight Custom ISA-Extended Secure Memory Subsystem for PicoRV32 RISC-V With AES Acceleration and Side-Channel Resilience

Authors: Koushik B, Ridhu Pharan A and Mohankumar N

Poster 15: Verification of UCIe Manageability Multi-Chiplet Systems: A Unified and Scalable UVM Methodology

Authors: Sushant Pathak, Deepak Nagaria, Vikas Makhija, Nagesh Mirgane and Nitesh Kumar

Poster 16: AI2: Accelerating Hardware Verification Through Intelligent Automation and Semantic Reasoning

Authors: Hardik Raina

Poster 17: Zero-Vulnerability Low-Power Verification: An Autonomous, Generic Framework for Eliminating Clock and Power Gating Bug Escapes

Authors: Debarati Banerjee and Nikhil Singla