

Tuesday, September 1, 2026						
Start	End	General Sessions - Grand Victoria				
9:00	9:15	DVCon India 2026 Welcome - Tutorial Day				
9:15	10:00	Vision Talk: Real Intent(Dr. Prakash Narain, President & CEO) - Transforming Static Sign-Off with Microarchitectural Analysis & AI				
10:00	10:30	Keynote Talk : NXP(Hitesh Garg, Vice President and India Managing Director of NXP Semiconductors) - Engineering at the Speed of Thought: AI-Driven Acceleration for the next gen designs				
10:30	11:00	Keynote Talk: Elinnos(Prabhu Bhairi, Founder & CEO, Elinnos) - Beyond Simulator + AI: AI-Integrated Simulation for Intelligent Verification				
11:00	11:30	Tea Break & Networking				
Start	End	Track 1 - Grand Victoria B	Track 2 - Grand Victoria A	Track 3 - Robusta & Arabica	Track 4 - Brain Box	Track 5 - Marquis
11:30	12:15	Tutorial TSW_1A: Siemens Agentic AI for RTL Signoff	Tutorial TSW_2A: Lubis EDA From Craft to System: A Platform Approach to Structured and Automated Formal Verification	Short Workshop TSW_3A_1: Verifast Tech VeriQuest – Redefining Design Verification through Agentic AI	Tutorial TSW_4A: Synopsys System Validation using Synopsys Interface Solutions	Design Contest 5A
12:15	13:00			Short Workshop TSW_3A_2: Cadence Agentic AI - Verification Flow		
13:00	14:00	Lunch Break				
14:00	14:45	Tutorial TSW_1B: Synopsys Scalable Formal Verification in the Era of AI	Tutorial TSW_2B: Accellera CDC-RDC Verification Standard 1.0 for Interoperable Abstract Model	Industry Discussion TSW_3B_1: HLS Assisted Architecture Exploration	Short Workshop TSW_4B_1: Synopsys Design Faster, Debug Smarter: AI-Enhanced Verification	Design Contest 5B
14:45	15:30			Academic Discussion TSW_3B_2: Can AI-enabled EDA transform Analog, Mixed-Signal and RF IC Design, or will it remain an expert-assistive tool?	Short Workshop TSW_4B_2: CDAC From Open ISA to Silicon: The RISC-V and VEGA Processor Journey	
15:30	15:45	Tea Break				
15:45	16:30	Tutorial TSW_1C: Accellera Sponsored: What's Cooking in SystemC 4.0 and Federated Simulation? Let's Be Friends	Industry-Academia Discussion TSW_2C: Open-Source chip design, flows & AI in Verification: Building an Open Ecosystem for Scalable Silicon Design	Short Workshop TSW_3C_1: Axiado Platform Intelligence Solutions - Design and Verification Perspectives	Tutorial TSW_4C: IEEE Standards Association and Accellera	Design Contest 5C
16:30	17:15			Short Workshop TSW_3C_2: Accellera's Portable Stimulus Standard: Examples and What's Next		
17:15	17:20	Day 1 Closing Remarks				

Exhibit Area Setup

EXHIBIT HOURS
10:30am to 5:00pm