Wednesday, September 2, 2026

Start	End						
		General Sessions - Grand Victoria					EXHIBIT HOURS 9am to 5:30pm
8:30	8:45	DVCon India 2026 - Conference Welcome & Inauguration					
8:45	9:30	Vision Talk: Siemens (*Abhi Kolpekwar, Senior VP & GM*) - The Future of Verification: One Path to Silicon Confidence					
9:30	10:00	Keynote Talk: Synopsys (*Pallab Dasgupta, Vice President of R&D Engineering, Synopsys*): Generative AI: Is it Real or Merely a Hallucination?					
10:00	10:30	Keynote Talk: Cadence (*Ziyad Hanna, Corporate VP, R&D*)					
10:30	11:00	Keynote Talk: Analog Devices (*Anil Kempanna, VP, Global Head of Digital Hardware Design*) - Intelligent Edge Needs a New Engineering Stack: Rethinking Architecture and Execution for Intelligent Physical Systems					
11:00	11:15	Tea Break & Networking					
Start	End	Track 1 - Grand Victoria B	Track 2 - Grand Victoria A	Track 3 - Robusta & Arabica	Track 4 - Brain Box	Track 5 - Marquis	
11:15	12:45	Paper Session 1A: SV & UVM / AI	Paper Session 2A: Static & Formal	Paper Session 3A: AMS & Low Power Design	Paper Session 4A: Design Architecture	Paper Session 5A: Functional Safety & Security	
11:15	11:45	1A1: AI-Augmented Constrained Randomized Framework with Feature-Specific Dynamic Customization for Lpddr6 based design Verification Coverage - by Dharini Subashchandran, Gruheshkumar Patel, Meghna Ahuja and Shyam Sharma	2A1: Control-Datapath Fusion: A Closed-Loop Formal Verification Case Study on Tensor Pipeline Architecture - by Shravya Jampana and Usha Rani Bagadi	3A1: Porting MBIST and SCAN Testbenches to Chip-Level in Analog-On-Top Designs: Enhancing DFT and Gate-Level Simulations - by Saranya Das	4A1: Task Aware Object Selection using Scene context Reasoning on Edge Hardware - by Avantika Somasundara Kumar Padma Devi, Adlin Rishana J and Shri Varshni N	5A1: Beyond Syntax: Ensuring the Safety and Style of AI-Generated Hardware - by Amarnath D	
11:45	12:15	1A2: AI Enabled Portable Stimulus Standard: Bridging the Gap Between Specification and Validation - by Kashish Jangid, Kaushal Modi and Ponnambalam Lakshmanan	2A2: Small Decomposition, Big Payoff: A Case Study on AI-Assisted Formal Verification of a Pipeline Intensive Retry Logic - by Sachin Kumawat, Arjun Singh and Amber Telfer	3A2: Left-Shift Power Estimation in SoC Design : Verification-Integrated Framework for Early Power Estimation Using Digital Mixed-Signal Simulation - by Isha Sharma and Amit Singh	4A2: The Tokens You Don't Need: Exploiting Video Compression for Faster VLM Inference - by Venkata Ajay Kolla and Suresh Vasu	5A2: RTL-Centric Safety Verification, A Staged Fault Injection Methodology from FMEDA to System-Level Sign-off Using Simulation and Emulation - by Nikhil Shivaprasad, Vedant Garg, Meera Ramani-Augustin, Alex Yap, Pritheshwar Thirugnanasambantham, Rohit Kumar and Lassaad Letaief	
12:15	12:45	1A3: LLM-Guided Closed-Loop Framework Development for Regression Reduction - by Aastha Sanjay Bhore, Arun Joseph and Binod Kumar	2A3: Spec to Bug Evidence: An Agentic AI Framework Accelerating Formal Verification Bug Discovery - by Devansh Shah, Neha Joshi and Anshul Jain	3A3: Power Sensitive Mixed-Signal Boundary Elements - by Pankaj Gairola, Anusriti Choudhuri and Serge Garcia-Sabiro	4A3: SIMD-Based Parallel Data Transfer for Low-Latency Systolic Array Acceleration in AI Workloads - by Yajjala Yamuna Kumari, Arun Nath K S, Divya D S, Krishnakumar Rao S	5A3: A Methodology for Adversarial and Systematic Concurrency-Aware Security Verification for Memory Protection of MPU/IOMMU Subsystems - by Sridhar Mukund, Prof Sastry Puranapanda, and Hemalatha Munnurukapu	
12:45	13:45	Lunch Break					
13:45	14:30	Industry Panel: Design Verification in the AI Era: Challenges, Opportunities, and Workforce Transformation in the 2030s Moderator: Nirmal Arumugam (Kandou AI), Panelists: Klaus-Dieter Hilliges (Advantest), Antonio Vaz (Quest Global), Pradeep Babu (Qualcomm), Harinagarjun Chippagi(TCS)					
14:30	15:30	POSTER HOURS					
15:30	15:45	Tea Break & Networking					
15:45	17:15	Paper Session 1B: SV & UVM / AI	Paper Session 2B: Static & Formal	Paper Session 3B: AMS & Low Power Design	Paper Session 4B: Design Architecture	Paper Session 5B: Functional Safety & Security	
15:45	16:15	1B1: AI Driven Regression Optimization and Coverage Closure with Cadence Verisium SimAI - by Vishnu G, Aravind R K, Krishna Priyanka Immidisetti and Sahadev Kumar	2B1: AI Agents for Data-Driven Reset Abstraction Decisions to Accelerate Formal Proof Convergence - by Anshul Jain, S R Pavitra, Sharika Shaju and Neha Joshi	3B1: SpecPro Modeller: An AI-Driven Framework for Automated Analog Behavioural Model Generation - by Sainath Karlapalem, Atish Savale and Vihan Shukla	4B1: Automated RTL Design Review driven by Microarchitectural Analysis - by Prakash Narain and Vinod Viswanath	5B1: Bridging the Gap: A Systematic Verification and Reliability Framework for Analog Compute-in-Memory Using GenAI-Driven Portable Stimulus - by Amarnath D	
16:15	16:45	1B2: Navigating the Cutting Edge: Strategic Verification of UFS5.0 in Next-Gen AI SoCs - by Premkumar Dhanabalan, Harsha Gollapalli, Shubham Garg, Shyam Sundar, Amitkumar Gound, Akshay R, Srinivasan T and Nikhil Sharma	2B2: FloatFix: An Agentic AI Debugger for Floating-Point Arithmetic in Formal Equivalence Verification - by Suraj Kamble, Mohit Choradia and Vichal Verma	3B2: Beyond Static Analysis: Improving Functional Coverage in Low Power Design Verification - by Arunav Goel, Sachin Bansal, M.Vaishnavi Reddy, Vishal Keswani and Manish Goel	4B2: Partition of large scale datacenter PCIe subsystem for faster turnaround and partition reusability - by Suraj Augustine, Sathish Sivakumar, Atul Chauhan, Ankush Nehra, Shibin Bose Kavara, Venkatesh Veluvolu, Akhil Goel and Rajat Verma	5B2: Securing Silicon from Birth: Preventing Zero-Fusing Attacks through Lifecycle-Aware Debug Verification - by Sourabh Tapas and Sreedhar Sankaramanchi	
16:45	17:15	1B3: NaSTR : Natural language specification to RTL Testbench generation with RAG models - by Ramya B T	2B3: Next-Gen Firmware Trust: Built on Formal, Scaled with AI - by Disha Puri, Aatreyi Bal and Sudipa Mandal	3B3: Design-Focused Feedforward Behavioural Modeling of PLL IPs for Fast SoC Verification - by Preeti Shukla and Amit Singh	4B3: PPA_CoPilot: An Agentic Framework for RTL Quality Analysis and PPA Optimization - by Srinivasa Sudhakar Tipparaju, Karun Kumar Talari, Yeshwanth Kumar Bandapally and Shruti Bheemanagoudra	5B3: On Security Signoff Experience at RTL driven by Minimally Boolean Static Analysis - by Vinod Viswanath and Varun Sharma	
17:15	18:30	Networking					
18:30	18:45	DVCon India 2026 Awards Welcome					
18:45	19:30	Industry Panel: Startup resurgence - Why it's a break out point for India. Moderator: Shivananda Koteshwar (AsterLabs), Panelists: Ujwala Reddy (Axiado), Ruchir Dixit (Siemens), Madhulima Tewari (VerifAIX Inc), Siddhant Dangi (Anthriq), Dheemanth Nagaraj (Agrani Labs)					
19:30	20:00	DVCon India 2026 Awards					
20:00	21:30	Dinner					