Tuesday, September 1, 2026						
Start	End	General Sessions - Grand Victoria				Exhibit Area Setup
9:00	9:30	DVCon India 2026 Welcome - Tutorial Day				
9:30	10:15	Vision Talk: Real Intent				
10:15	10:45	Keynote Talk: NXP				
10:45	11:15	Tea Break & Networking				
Start	End	Track 1 - Grand Victoria B	Track 2 - Grand Victoria A	Track 3 - Robusta & Arabica	Track 4 - Brain Box	EXHIBIT HOURS 10:30am to 5:00pm
11:15	12:00	Tutorial 1A: Siemens	Tutorial 2A: Lubis EDA From Craft to System: A Platform Approach to Structured and Automated Formal Verification	Short Workshop 3A_1: Verifast Tech	Short Workshop 4A_1:	
12:00	12:45			Short Workshop 3A_2: IEEE	Short Workshop 4A_2:	
12:45	14:00	Lunch Break				
14:00	14:45	Tutorial 1B: Synopys Scalable Formal Verification in the Era of AI	Tutorial 2B: Accellera CDC-RDC Verification Standard 1.0 for Interoperable Abstract Model	Short Workshop 3B_1: Cadence Agentic AI - Verification Flow	Short Workshop 4B_1:	
14:45	15:30			Academic discussion 3B_2: Can AI-enabled EDA transform Analog, Mixed-Signal and RF IC Design, or will it remain an expert-assistive tool?	Short Workshop 4B_2:	
15:30	16:00	Tea Break				
16:00	16:45	Tutorial 1C: Synopsys System Validation using Synopsys Interface Solutions	Industry-Academia Discussion 2C: Open-Source chip design, flows & AI in Verification: Building an Open Ecosystem for Scalable Silicon Design	Short Workshop 3C_1: Synopsys Design Faster, Debug Smarter: AI-Enhanced Verification	Short Workshop 4C_1:	
16:45	17:30			Short Workshop 3C_2:	Short Workshop 4C_2	
17:30	17:35	Day 1 Closing Remarks				