

Thursday, September 3, 2026					
Start	End	General Sessions - Grand Victoria			
9:00	9:15	Welcome & TPC Update			
9:15	10:00	Vision Talk: Axiomise (Ashish Darbari, Founder & CEO) : Proof, Not Prompt: Why AI Silicon Needs Formal Verification, Not Just AI-Generated Assertions			
10:00	10:45	Industry Panel: From Classroom to Chip Design: Preparing the Workforce for the Semiconductor-AI Era Moderator: Ramanujam Thodur(Texas Instruments), Panelists: Ameya Pangarkar (Astera Labs), Sreenu Yerabolu (Lancesoft), Priya Ananthakrishnan (Mirafr)			
10:45	11:15	Industry Talk: Prodigy Techno (Vibhav Kaki, Sr. Software Engineering Manager) : Bridging Pre-Silicon Verification to Post-Silicon Debug with Protocol-Aware Tools			
11:15	11:45	Tea Break & Networking			
11:45	13:15	Track 1 - Grand Victoria B Paper Session 1C: SV & UVM / AI	Track 2 - Grand Victoria A Paper Session 2C: Static & Formal	Track 3 - Robusta & Arabica Paper Session 3C: SV & UVM	Track 4 - Brain Box Paper Session 4C: RISC-V Design & Verification
11:45	12:15	1C1: ML-Driven Automated Functional Verification Framework for Digital Designs - by Laxmikant Chavan and Dr Madhura R	2C1: Autonomous Formal Sign-off: Scaling High-Radix Crossbars Verification via GenAI and RPD Synthesis - by Aman Vyas and Nitin Ahuja	3C1: Analytical Framework for Optimal Sample Point Delay Calculation for Signal I/O Buffers - by Arpit Saxena, Gaurav Jain, Dharini Subashchandran and Shyam Sharma	4C1: Directed Adaptive Stimulus Evolution (DASE): Coverage-Directed Evolutionary Stimulus Generation for RISC-V RTL Verification - by Ankush Kumar Jaiswal, Aarav Sharma, Garvit Maheshwari and Jean Jenifer Nesam
12:15	12:45	1C2: FunCovr.ai: AI that Generates Sharper Coverage & Smarter Closure - by Mahesh Shinde, Shashivardhan N A, Avinash Anantharamu, Nitin Neralkar and Veeraraju Potta	2C2: Debug Assist: An LLM-Guided Framework for Debugging FPV Failures - by Kevin Bhensdadiya, Vichai Verma and Ajay Kumar Kolluri	3C2: FirmScope: Post-Simulation Firmware Debug from Waveforms, PC Traces, and Source Code - by Pradeepkumar Santdasani, Prashant Sharma and Digvijaya Singh	4C2: System-Level Verification of N-Trace for a Family of RISC-V Cores - by Nikhil Jain, Kshitij Sukhwai, Jay Gamoneda and Sourav Roy
12:45	13:15	1C3: Deterministic Generative AI Framework for Context-Aware Verification Testbench Generation - by Govarthanam Krishnasamy	2C3: FUSION: Formal verification Using Spec-aware Integration for Optimization - by Bhanu Pratap Singh, Moola Jeevan Chaitanya Goud and Sakthivel Ramaiah	3C3: Reimagining Design Verification: Skilling up the game - by Yaswani Priyanka Vempali and Rajiv Hasija	4C3: Reconfigurable Automated SVA Generator for DFT Validation - by Hemanth Sekhar Kothapalli, Adithya Rangan Ck, Murugeswaran Surulivel, Sivasaravanan R and Kali Mani S
13:15	14:15	Lunch Break			
14:15	15:15	POSTER HOURS			
15:15	15:30	Tea Break & Networking			
15:30	17:00	Paper Session 1D: SV & UVM / Debug	Paper Session 2D: Chiplet Verification	Paper Session 3D: SV & UVM	Paper Session 4D: RISC-V Design & Verification
15:30	16:00	1D1: From Prompt to Probe: Left-Shifting SoC Debug with Generative AI - by Gaurang Goyal, Ravi Mangal, Debraj Dutta and Jaideep Ramesh	2D1: Multi Die Verificaiton Flow and Methodology - A case study - by Venkata Markandeyulu Boddu	3D1: Accelerated verification sign-off: Delta code review and Incremental Coverage Workflow using Synopsys RTL-TRACE - by Bholendra Pratap Singh, Garima Singh and Aravind R K	4D1: Edge-Efficient Context-Aware Object Detection - by Poojaa Sri S, Rishivathen C and Abishek S
16:00	16:30	1D2: CoCorA : An efficient RTL Code debug and Correction Assistant - by Ramya B T	2D2: Agentic AI-Driven UClE IIP-VIP Integration: Accelerating Chiplet Verification - by Divya Jindal	3D2: Software-Informed Constrained Random Testing: Bridging HW/SW Co-Design and Verification via Temporal Workload Signatures - by Amarnath D	4D2: AI-Driven Coverage-Directed Smoke Regression Optimization via Greedy Set Cover for RISC-V Verification - by Anish Jaitare, Abhishek Rajgadia, Shubham Singla and Radha Govindaradjou
16:30	17:00	1D3: CLOSED-LOOP DEBUG AGENT: SIMULATION-GATED JOURNAL CONFIRMATION - by Atif Afzal and Meras Pillai Rashid	2D3: Taming AXI Complexity over UClE: Beyond Protocol Compliance with a Scalable, Configuration-Driven Verification Framework - by Gunjan Kumar Gupta, Sandeep Kumar Chintala, Venkatesh Kudumula, Tai-Jhou Chen and Ray Varghese	3D3: Verification-Driven Interface Convergence: Methodology for Validating Functional Interoperability And Accelerating Subsystem Design for Concurrently Developed Compute and Component IPs in Coherent Subsystems - by Alisha Parvez, Preethi Ashok Kumar, Shreya Singh, Jyothi Kumari and Rohit Jindal	4D3: AI-Driven RTL Change-Aware Testlist Generation for RISC-V Core Verification - by Vikas Dubey, Abhishek Rajgadia, Shubham Singla and Radha Govindaradjou
17:00	17:30	Best Paper Awards & Closing			

EXHIBIT HOURS

9am to 5:30pm